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Fast Carry Logic for Digital Computers*

BRUCE GILCHRIST†, J. H. POMERENE†, AND S. Y. WONG‡

Summary—**Existing large scale binary computers typically must allow for the maximum full length carry time in each addition. It has been shown that average carry sequences are significantly shorter than this maximum, on the average only five stages for a 40 digit addition. A method is described to realize the implied 8 to 1 time saving by deriving an actual "carry completion" signal. Experimental results verify this saving.**

Introduction

A NEED HAS been shown[1] for significantly higher computational speeds than are afforded by existing machines. Although the term speed as here used should perhaps be viewed in the most general sense, that is, a speedup of the whole process intervening between the statement of a problem and its final solution, at least some speedup should be expected to come from a decrease in the execution time of the elementary machine operations, combinations of which form the basic arithmetic and logical processes. The carry process arising in the parallel addition of numbers, which is essentially serial, is one such elementary operation. A method is given for significantly decreasing the time required for the carry process by using the average properties of carry sequences. Such a method is of particular interest not just for the addition operation itself, but also for the possibility of speeding up the ordinary repeated addition type of multiplication. It would be of great value if this simple type of multiplication could be performed in a time comparable with simultaneous multiplication, which is potentially fast, but costly in equipment.[2]

We distinguish the carry propagation, which is serial, from the formation of the sum digit, which is parallel, given the carries. Thus assuming the addends to be applied simultaneously to the N parallel stages of the adder at time t_0, we observe the carry into the most significant stage of the adder and call the time t_1 when it recognizably assumes its final value. We define the N stage carry time to be $NC=t_1-t_0$ when the carry arises at the least significant stage and progresses through to the most significant. At least a majority of existing machines employ carry circuits in which the full length carry time NC must necessarily be allowed in each addition. The required time allowance is typically provided by a separate timing device such as a multivibrator. The actual time provided must be NC plus a safety margin to allow for tolerances in both the carry circuit and the timing device.

In practice this safety margin may be an appreciable fraction of NC. Every designer of an asynchronous machine has probably considered using the carry circuit to time its own full length carry time NC. One such method is given by Richards[3] and a similar method is also embodied in the logic to be described. These methods certainly increase the timing reliability of the carry system and also save above mentioned safety margin.

A more significant speedup can be made if time is allowed only for the actual carries arising in the particular additions. In an early discussion of the logical design of a computer,[4] it was shown that on the average the maximum length of a 1's carry sequence in a 40 digit addition is only 4.6 stages. If fully exploited, this result could lead to an 8-fold saving in average carry time. Such a saving, resulting from logic alone, has the important property of being additional to that resulting from faster components. The logic to be described gives almost this 8-fold saving. It differs from the optimum because carry sequences of 0's as well as 1's must be considered and in this case the average maximum carry sequence is shown to be 5.6 stages.

C_{in}	A	B	C_{out}	
0	0	1	0	
0	1	0	0	carry out is determined
1	0	1	1	by carry in
1	1	0	1	
0	0	0	0	
1	0	0	0	carry out is determined
0	1	1	1	solely by the addends
1	1	1	1	A, B

Fig. 1—Truth table for carry determination.

Fig. 1 shows the truth table for determining the output carry, C_{out}, for one stage of a binary adder, the inputs to which are the addends A and B and the input carry C_{in}. The eight input combinations are divided into two groups of four each, according to whether or not the output carry can be stated independently of the input carry. We establish our nomenclature by considering first the simple carry determination logic given in Fig. 2. Here the symbol $(\overline{00})$ means that A and B are not both zero, while (11) means that both A and B are one's. C^1 indicates a carry of one.

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[1] The numerical weather prediction problem is an example of this; e.g., B. Gilchrist, "Computers and weather prediction," *Comp. & Autom.*, vol. 4, pp. 8, 9; March, 1955.

[2] R. K. Richards, "Arithmetic Operations in Digital Computers," D. Van Nostrand & Co., New York, pp. 138–140; 1955.

[3] R. K. Richards, op cit.

[4] A. W. Burks, H. H. Goldstine, and J. von Neumann, Preliminary discussion of the logical design of an electronic computing instrument, 1947.

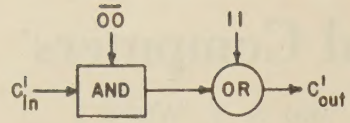


Fig. 2—Simple carry logic.

This simple carry circuit is incapable of providing its own timing because of the carry interruptions (caused by 00) and carry starts (caused by 11) which may occur variously throughout the N stages. A symmetrical treatment involving also 0 carries (C^0) as in Fig. 3 results in a circuit which can provide its own timing. Essentially a separate carry chain is provided for the 1's and for the 0's. The state of the carry lines should now be viewed as "off" or "one" for C^1 and "off" or "zero" for C^0. At the beginning of an addition, both carry lines are "off." This condition will be met if both carry inputs to the least significant stage are held "off."

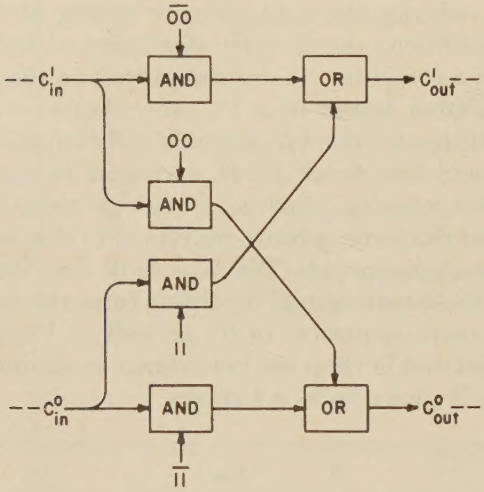


Fig. 3—Logic for self-timing full length carry.

The carry sequence is begun by setting one of these inputs, say C^0, to the "on" state. This carry will then proceed down the "0" chain until it reaches a stage having (11), where the carry switches over to the "1" chain. Similarly, it will then proceed down the 1 chain until it reaches a stage having (00), where it will switch back to the zero chain. Finally it will emerge from the most significant stage as either a C^0 or a C^1 to signal the end of the N stage carry. This zig-zag process is indicated schematically in the upper part of Fig. 4 which traces the carry chains through ten stages of an adder with the given addends A and B. It should be emphasized that the carry will always pass serially through ten stages although the route will be determined by the addends.

The Logical Circuit

A re-examination of Fig. 1 in the light of this circuit leads to the logic for deriving a completion signal for the actual carries. The first four cases are seen to be the ones for which the output carry depends on the input

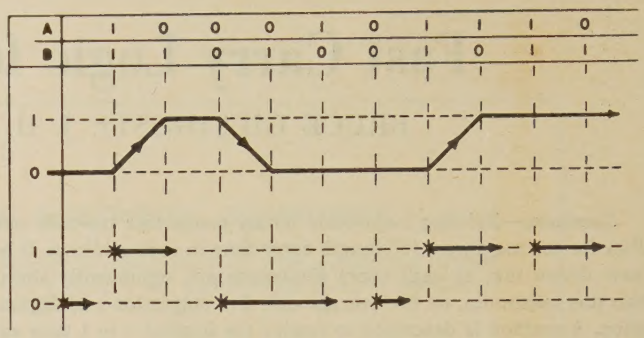


Fig. 4—Carry sequences in ten consecutive adder stages with addends A and B. Upper sequence is for logic of Fig. 3 and lower sequence is for logic of Fig. 5.

carry, while in the latter four cases the output carry is independent of the input. This result is used in the logic shown in Fig. 5. The dual carry chains of the previous circuit have been retained but the C_{in} restrictions on (11) and (00), that is, the cross connections, have been deleted. An N input "and" gate has been added to signal the presence of a carry (1 or 0) at each of the 40 stages. As before, both carry lines are off at the start of an addition, this being enforced for the interior stages by an explicit parallel inhibition on the lines or by operating on the 11 and 00 inputs. Carries are begun by releasing the inhibitions on all stages, including the selected carry into the least significant stage. At this moment carry sequences will arise from the selected input carry, and from every interior stage having (00) or (11). Thus the serial aspect of the carry is restricted to sequences of stages for which $A \neq B$.

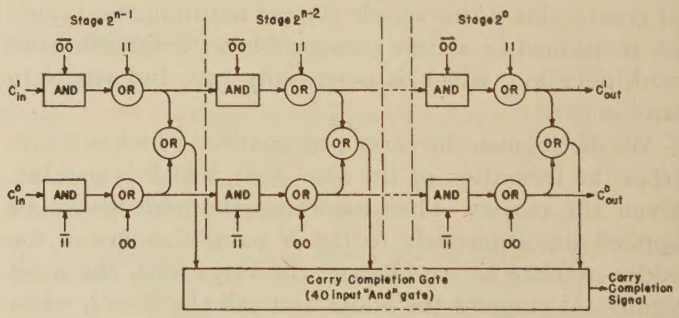


Fig. 5—Logic for self-timing actual carries.

The lower half of Fig. 4 shows the carry chains resulting for this final circuit using the same addends as previously. Six carry sequences are started simultaneously as marked by the asterisks. Since for these marked stages the input carry is irrelevant to the output carry, incoming carry sequences stop at the stage just prior. Now it is seen that for this example the longest carry sequence is three stages instead of the full ten. For the more practical case of 40 digit numbers, it is shown below that the average longest carry sequence will be 5.6 stages. Thus after an average time delay of only 5.6 C each of the 40 inputs to the carry completion gate will be enabled, signalling the end of the carry process.

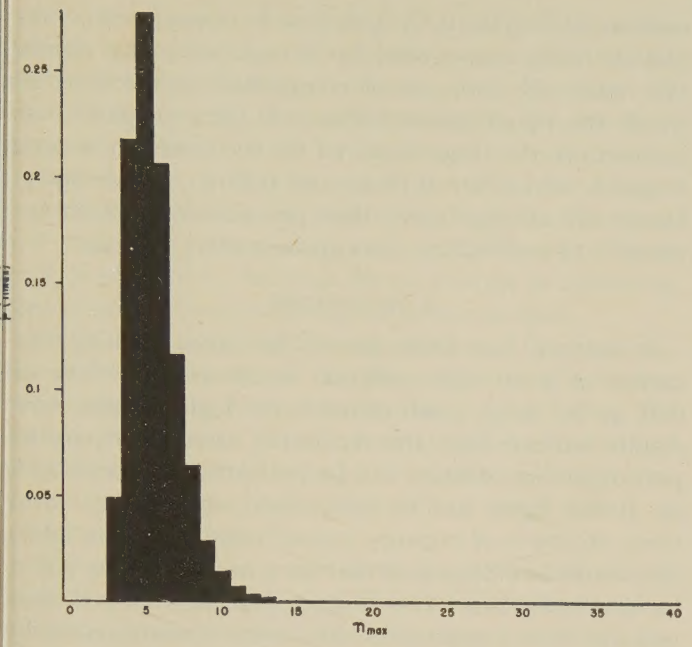


Fig. 6—Probability distribution of the maximum length carry sequence (n_{max}) arising in a forty digit addition.

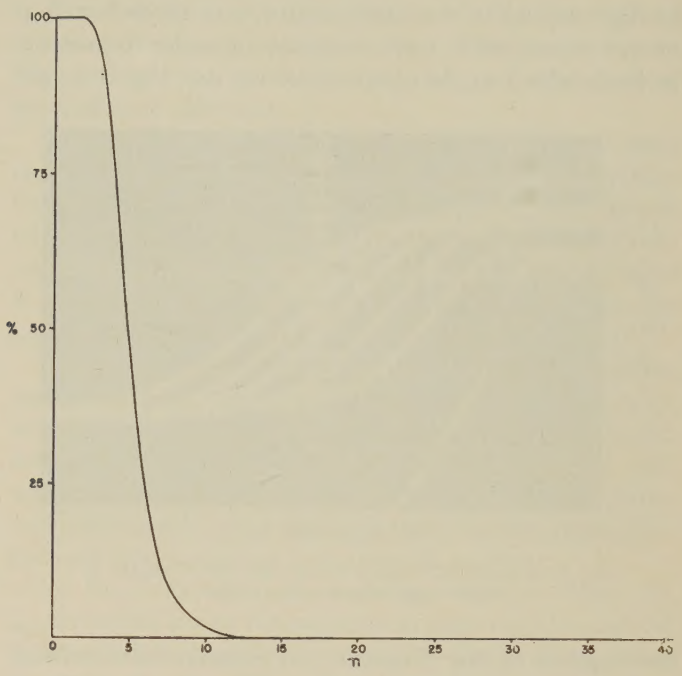


Fig. 7—Percentage of additions having a maximum length carry sequence greater than n.

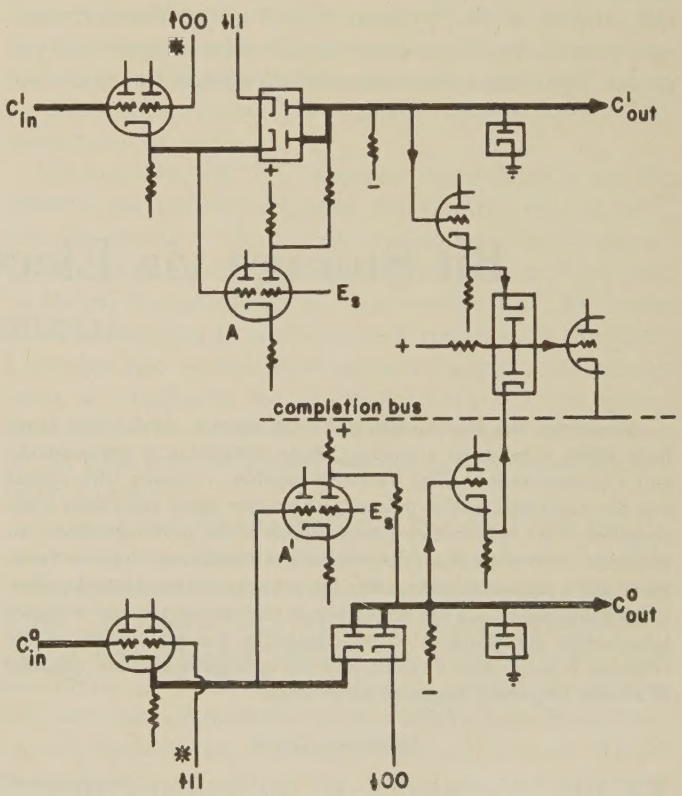
Properties of Carry Sequences

The analytic approach of Burks *et al*[5] to the problem of determining the properties of 1's carry sequences is unable to give more than the value of the average maximum carry sequence and gives no information as to the variance of this maximum carry. Thus, while in principle we could have extended this analytic approach to include the present case of both 0 and 1's carry sequences, it was decided to obtain the results by actual numerical experiment so as to gain some knowledge as to the variance.

A code was therefore written for the IAS computer to examine the properties of carry sequences. This code generates pairs of random 40 digit numbers and adds them digit by digit to obtain for each pair of numbers the maximum carry sequence (n max) of 1's or 0's arising. The distribution of n max found from 4,000 random additions is shown in Fig. 6. The distribution was unchanged by increasing the sample size. From these results the average maximum carry length, defined as $\sum_{n\max} P(n_{\max})$. $n_{\max}$ was found to be 5.6. It is of interest to note the small deviation of the individual maximum carry length from this average. This is brought out by Fig. 7 which shows the percentage of additions which have a maximum carry sequence greater than n.

It seemed desirable also to check the carry sequence properties of the interior additions involved in the simple multiplication process mentioned earlier. Using a similar code to that for examining addition it was found that the average maximum carry length was again 5.6. Thus in a typical multiplication of two forty-digit numbers the average sum of the individual maximum carries will be $20 \times 5.6 = 112$.

[5] A. W. Burks, H. H. Goldstine, and J. von Neumann, loc. cit.



* parallel carry turn-off also
$E_s \approx -5$ volts. Tubes A&A' restandardize carry as needed.

Fig. 8—Per-stage carry circuit of experimental adder.

Experimental Results

An eight stage experimental accumulator was constructed embodying the carry logic described above. The per-stage circuit for the carry portion is shown in Fig. 8. It should be noted that the circuits providing

the digit inputs to the carry circuit, and those forming the new sum from it, were connected in order to present the loads which would obtain in actual use. Fig. 9 shows

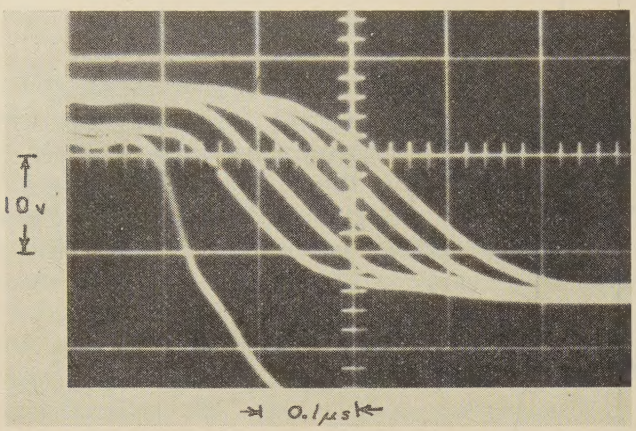


Fig. 9—Completion signals for several carry lengths in eight stage experimental adder.

the response of this circuit to carry sequences of several different lengths. In each case carries were started by enabling the carry lines and the carry input C^0 to the least significant stage and observations were made at the output of the 8 input "and" gate. The leftmost curve shows the carry start signal and successive curves to the right show the completion signals for carry sequences of lengths 0, 2, 4, 6, and 8, respectively, completion being represented by a negative going signal. We define the moment of completion as the time at which the signal passes below -5 volts. Of particular interest are the times required for the carries of length 4 and 6, which are 0.18 μs and 0.22 μs, respectively. Hence the average carry time per addition will lie between 0.18 and 0.22 μs, or approximately 0.21 μs.

Conclusions

A method has been shown for accomplishing the carries of a 40 digit addition in an average time of 0.21 μs by using a self-timed carry logic. Preliminary results indicate that the remaining essentially parallel portion of the addition can be performed in about 0.15 μs. If this figure can be maintained, the average total time, exclusive of memory access, required for an addition could be 0.36 μs and that for a multiplication could be $40 \times 0.15 + 20 \times 0.21 = 10.2$ μs. The carry circuit used requires more components than carry circuits generally used, but the significant increase in speed offsets the increased complexity. In addition, the inclusion of the 40 stage "and" gate permits a carry-less determination of the equality of two addends, this mode being obtained by not releasing the parallel carry inhibitions shown in Fig. 8. In this case an output is obtained from carry completion gate if, and only if, two addends are equal.

Bit Storage via Electro-optical Feedback*

ALFRED MILCH†

Summary—**An electro-optical binary storage device has been built which consists of a vacuum diode containing a photocathode and a phosphoranode. The device is capable of storing both optical and electrical information pulses. The present paper comprises a description of the behavior and construction of the prototype diode, an empirical derivation of a criterion for the conditions of stable feedback, and a numerical calculation for the case of two electrode pairs. Briefly mentioned are the possibility of high speed storage of digital information, the problem of self-triggering, the applicability of the criterion to solid state devices, and the analogous bistable behavior of a radio frequency triggered neon diode.**

Introduction

THE FACT which makes contemporary high speed digital computing machines possible is that electrons are low-inertia entities which may be conveniently transferred from one place to another. Photons enjoy the same advantage and, in some ways, are easier to transport than electrons. In addition, an optical information pulse may readily be converted to an electrical information pulse, and vice versa. There is thus the possibility that optical and electrical information pulses, used cooperatively, may lead to important advances in digital data processing. One way in which this may be done would be to incorporate a photosensitive cathode and a cathodoluminescent anode in a single vacuum envelope. This idea is of rather recent conception, and to this writer's knowledge, it originated as an "image transformer"[1] in 1934. Its contemporary descendent, the image converter tube, is finding wide application as an electro-optical transducer.

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† Mellon Institute, Pittsburgh, Pa.

[1] G. Holst, J. H. DeBoer, M. C. Teves, and C. F. Veenemans, "Transformation of light of long wavelength into light of short wavelength," *Physica*, vol. 1, pp. 297–305; 1934.

One of the main attractions of photons as information carriers is the fact that they may be transported through space directly. Thus an ordinary lens becomes the equivalent of a multichannel transmission line. Furthermore, in a device such as an image converter tube, equipped with deflection plates or coils, the images representing information pulses may be shifted in space, and delayed in time, in a very versatile way. These general ideas form the basis for an interest in exploiting optical phenomena in the digital computer field.

As far as making specific recognition of the possibilities of feedback between the elements of such a device, there appears to have been nothing done except for certain preliminary experiments at this Laboratory,[2,3] plus other incidental remarks in papers on image converter tubes regarding precautionary steps taken to avoid such feedback.[4,5]

The present paper proposes to show that not only is such feedback possible, but that by including an RC network in the external circuitry, true bistability becomes possible. In addition, this paper will describe the behavior of a prototype tube built to foster feedback, and will demonstrate that an exact expression for the conditions of feedback equilibrium is available, based upon the individual properties of the photocathode and phosphoranode. The approach will be quite empirical in that the fundamental nature of the processes occurring within the active elements will be ignored in favor of using operational characteristics as determined experimentally.

Behavior of a Bistable Vacuum Photodiode

The electrode pair chosen for this work was the manganese activated zinc silicate phosphor screen (P1 type) and a silver-oxygen-cesium photocathode (S1 type). Unfortunately, experimental difficulties encountered involving the great chemical sensitivity of the phosphor screen to the cesium vapor allowed, in the time available, the construction of only one such tube. This is described below.

At low voltages (ca. 250 volt) this diode behaved like an ordinary phototube with a wire anode. Its dark current was linear, and it exhibited current saturation, although not as sharp as its commercial counterpart—the RCA type 922. At higher voltages the tube shows sharply different behavior in that no current saturation is shown and the tube will store; that is a voltage is reached above which a pulse of light will cause a current to flow and the anode to emit light, which effects persist without decay after the initiating pulse has vanished. Fig. 1 shows the conduction curves and storing characteristics of this tube.

When the external circuit contains only a load resistor, it is necessary to decrease the applied voltage below the sustaining level to cause the tube to switch off. In the context of this paper, this is outside the definition of true bistability. Bistability will be exhibited if and only if a suitable capacitor is placed across the load resistor [see Fig. 1(b)].

A relatively weak pulse of illumination, P_1, falling on the cathode causes a correspondingly small photocurrent, i_1 to flow. This current, impinging on the anode, results in a feedback so that as long as the applied voltage is not reduced below a critical value, a current flows and the anode emits a continuous visible glow after the initiating radiation has dropped to zero.

To turn the tube off, a strong pulse of light, P_0, is allowed to strike the cathode so that a heavy current is observed at A while the voltage V (tube) drops below the critical value. When P_0 is removed, the capacitor C comes into play, holding the voltage low until the anode glow is insufficient to re-excite the cathode. Thus a capacitor C must be chosen so that the RC constant is long enough to outlast the slowest process involved here. These conditions have also been met, using an arbitrarily chosen 150 megohm resistor and a 0.01 microfarad capacitor.

Intrinsically, the RC constant depends only on the speed of the cathode response, the electron transit time, and the speed of the phosphor response. Inasmuch as two tungsten filament lamps of different intensities were employed for switching, the time constant of $1\frac{1}{2}$ seconds bears no relation to the frequency response of the tube. Likewise, the vertical lines are not realistic, but merely serve to emphasize the sequential nature of the operations indicated. Because of the above behavior, the state of the tube may be sensed and controlled either electrically or optically.

It turns out that an ordinary gas diode behaves in an exactly analogous manner. Experiments in this Laboratory have shown[6] that if a neon diode is "illuminated" by pulsed radio frequency energy applied to a coil of wire wrapped around the tube envelope, true bistability is obtained, provided, of course, the proper RC network is included. Fig. 2 shows typical conduction curves and storing characteristics of a type NE-96 neon diode.

A Criterion for Feedback Equilibrium

Consider a device containing a phosphoranode and a photocathode at an applied voltage, V. Assume that

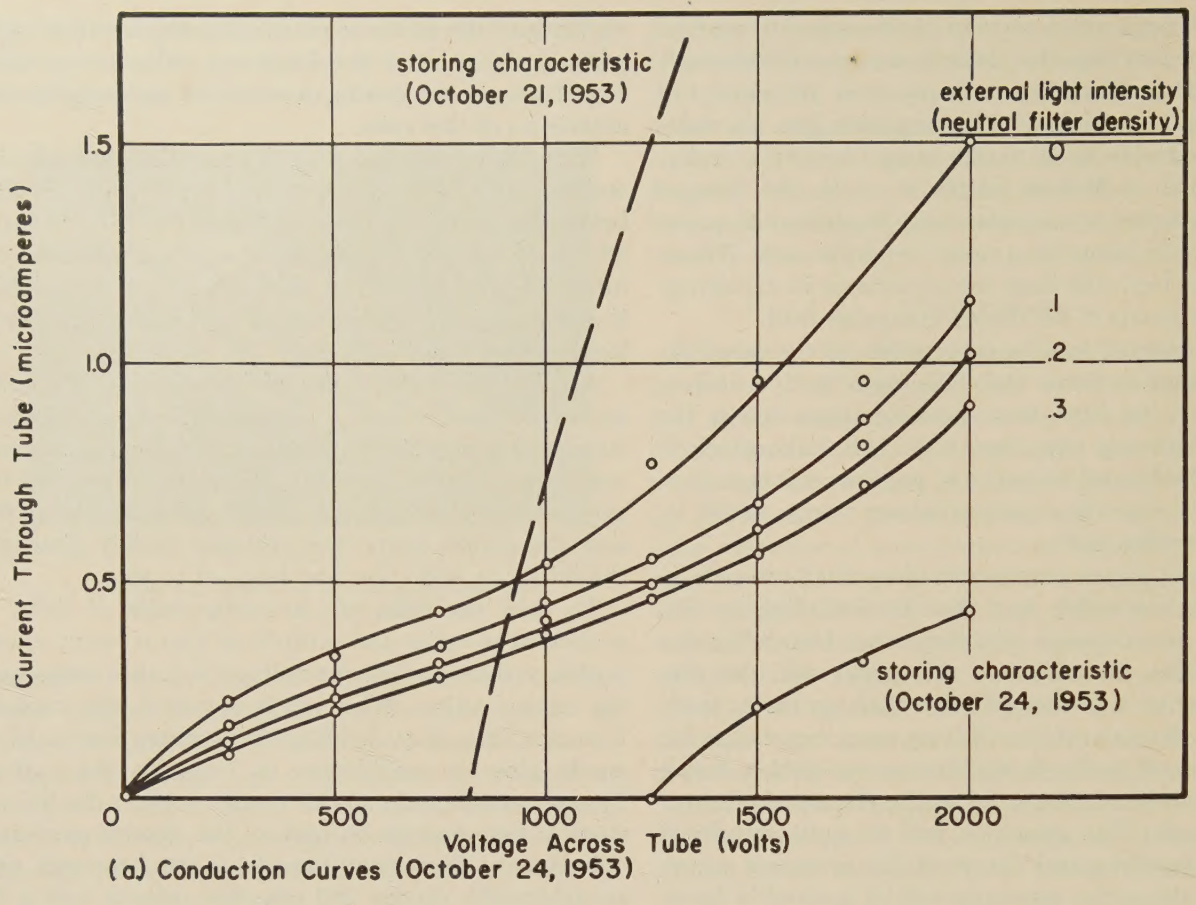
[2] J. R. Bowman, F. A. Schwertz, and B. O. Marshall, "Optical components for digital computers," Quarterly Report No. 3, Computer Components Fellowship, Mellon Institute; August, 1951.

[3] A. Milch, "Bistable optical storage system," pp. 129–134, Proceedings, 1954 Electronic Components Symposium, Washington, D. C.

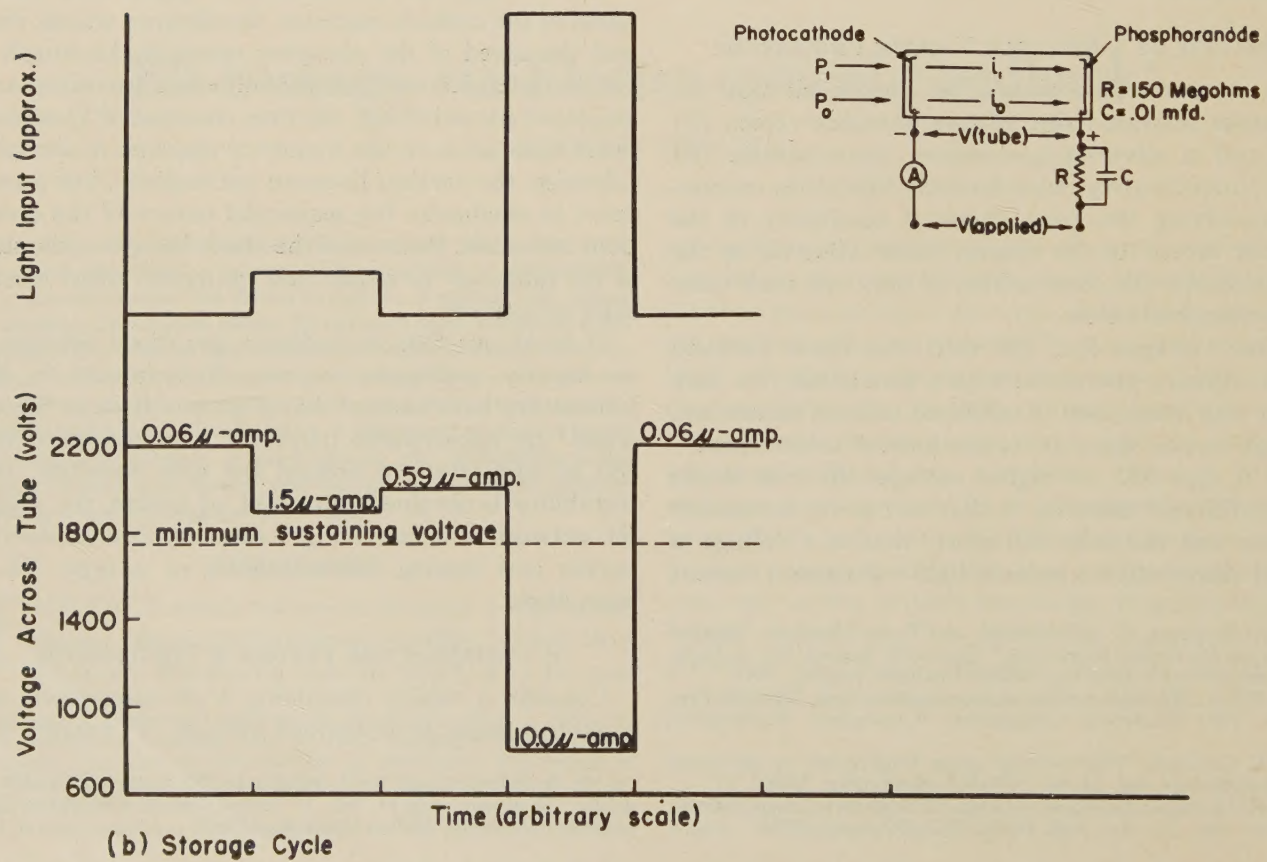
[4] J. W. Coltman, "Fluoroscopic image brightening by electronic means," *Radiology*, vol. 51, pp. 359–367; September, 1948.

[5] R. K. Orthuber and L. R. Ullery, "A solid state image intensifier," *Jour. Opt. Soc. Am.*, vol. 44, pp. 297–299; April, 1954.

[6] F. A. Schwertz and R. T. Steinback, "Rf triggered bistable gas diode," Quarterly Report No. 1, Second Series, Computer Components Fellowship, Mellon Institute; 1953.

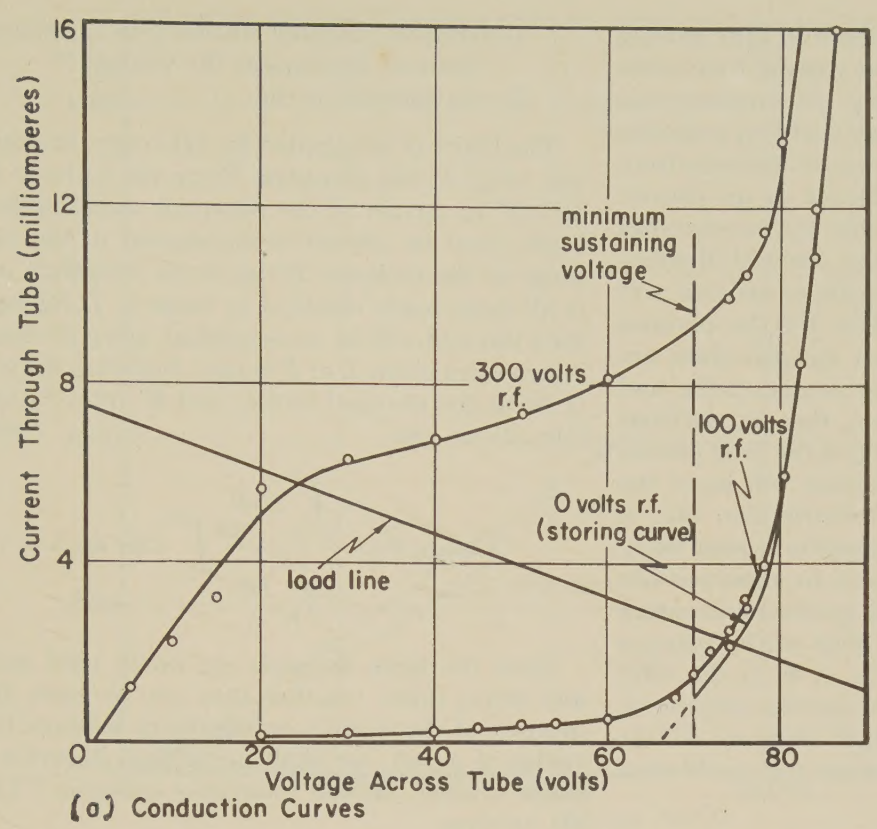


(a) Conduction Curves (October 24, 1953)

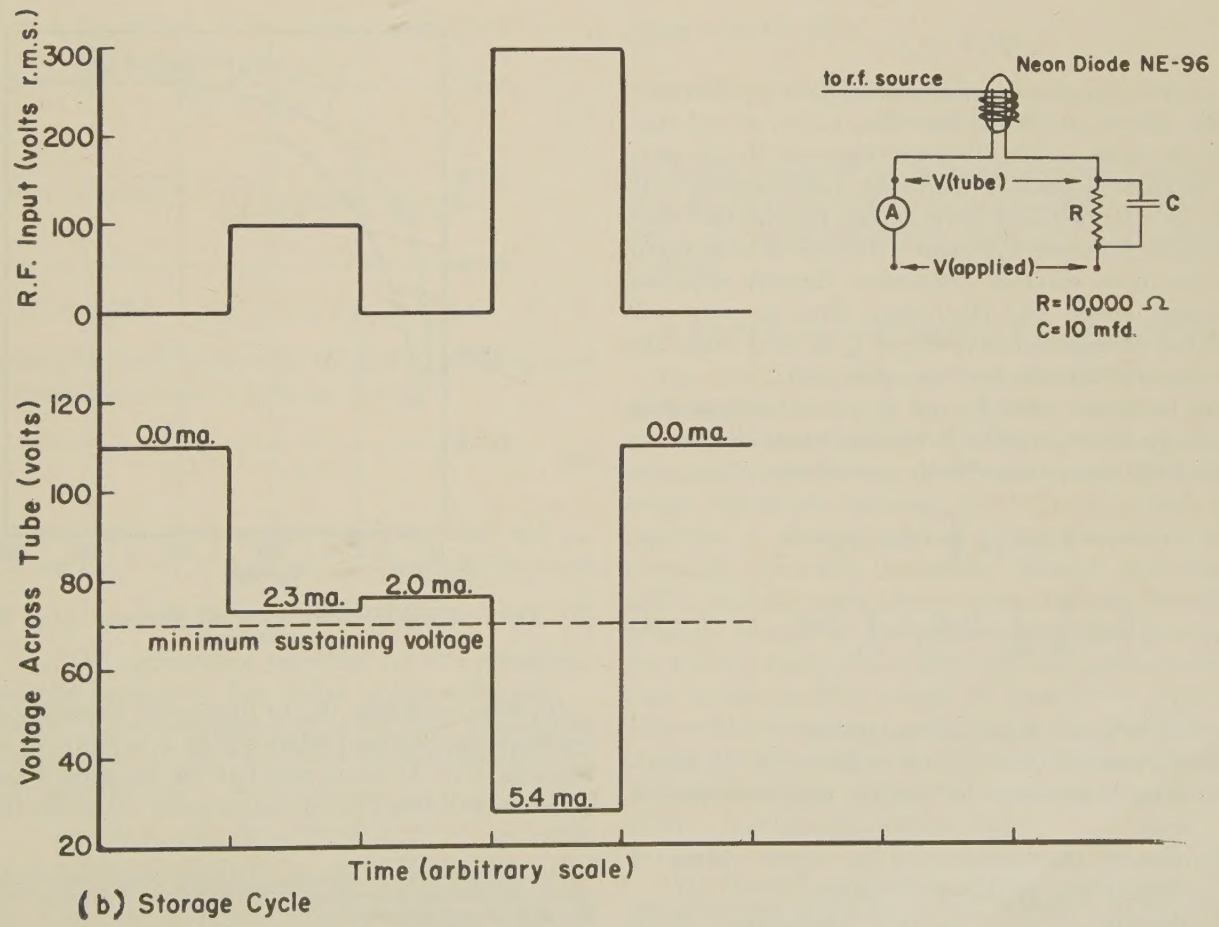


(b) Storage Cycle

Fig. 1—Optically triggered bistable vacuum diode (Pi-Si type).



(a) Conduction Curves



(b) Storage Cycle

Fig. 2—Radiofrequency triggered bistable gas diode (NE-96).

for at least one instant of time, there is light passing from anode to cathode and current passing from cathode to anode. Without considering the fundamentals of the phenomena themselves, we see that four processes must occur simultaneously: (a) transit of electrons from cathode to anode under the influence of an electric field, (b) penetration of the phosphor by the electrons to produce photons having a certain spectral distribution, (c) transit of photons from anode to cathode, and (d) penetration of the photosurface by the photons to produce electrons. If at a given moment there are α electrons per second leaving the photocathode, and if the electron transit efficiency is t_e, then αt_e electrons per second will strike the anode. If Q is the total photon yield of the anode, then $\alpha t_e Q$ photons will leave the anode. They will have a spectral distribution that is characteristic of the particular phosphor screen being considered. If t_p is the transit efficiency for these photons which we shall assume to be purely geometric in nature and independent of wavelength, then $\alpha t_e Q t_p$ photons will arrive at the cathode. Finally, if Φ' is the total quantum yield of the cathode to the spectral output distribution of the anode, then $\alpha t_e Q t_p \Phi'$ electrons will be leaving the cathode. The requirement for equilibrium is that

$$\alpha t_e Q t_p \Phi' = \alpha \tag{1}$$

or

$$t_e Q t_p \Phi' = 1. \tag{2}$$

Eq. 2 is the general criterion for feedback equilibrium, for if the above product is less than unity, α will continually decrease, as will all other tube activity, to zero. If the product is greater than one, tube activity will tend to increase without limit except for the fact that the increasing current will cause a voltage drop to occur across the finite external resistance, thereby reducing the voltage across the electrodes. This in turn will depress the voltage-sensitive factor Q (4) and cause the product on the left side of (2) to seek unity.

It can be shown that Φ' and Q can be expressed in terms of the more readily available quantities, sensitivity and efficiency respectively, as follows:

$$\Phi' = 2.3KS_{\max} \int_{\lambda_1}^{\lambda_2} LRd \log \lambda \tag{3}$$

$$Q = \frac{Vf}{K} \int_{\lambda_3}^{\lambda_4} L\lambda d\lambda \Big/ \int_{\lambda_3}^{\lambda_4} Ld\lambda \tag{4}$$

where

$K = hc/10^7\epsilon$, fundamental constants

$S_{\max}$ = photosensitivity at the wavelength of maximum sensitivity in (micro) amperes/(micro) watt

R = relative photosensitivity for equal values of radiant flux at all wavelengths

f = absolute intrinsic phosphor efficiency

V = the accelerating voltage

L = relative phosphor efficiency to a monoenergetic beam of electrons at the voltage V

λ = wavelength in cm.

The limits of integration for (4) cover the entire output range of the phosphor. Since the cathode may be "blind" to certain of the phosphor wavelengths, these limits must be altered to correspond to the visibility range of the cathode. If the limits for $\int L\lambda d\lambda$ only are in all cases made identical to those of $\int LRd \log \lambda$ (3), then this end will be accomplished, since obviously LR is zero when either L or R is zero. Inserting the values of Q (with the changed limits) and Φ' from (3) and (4) into (2) we get

$$2.3fS_{\max} Vt_p t_e \frac{\int_{\lambda_1}^{\lambda_2} L\lambda d\lambda}{\int_{\lambda_3}^{\lambda_4} Ld\lambda} \int_{\lambda_1}^{\lambda_2} LRd \log \lambda = 1. \tag{5}$$

Since the three integrals are rarely used explicitly, and since, taken together they are to some degree a measure of the relative compatibility between the electrodes of a pair, we shall lump them together into a single symbol, M, the "matching constant." Thus the (5) becomes

$$2.3fS_{\max} Vt_p t_e M = 1. \tag{6}$$

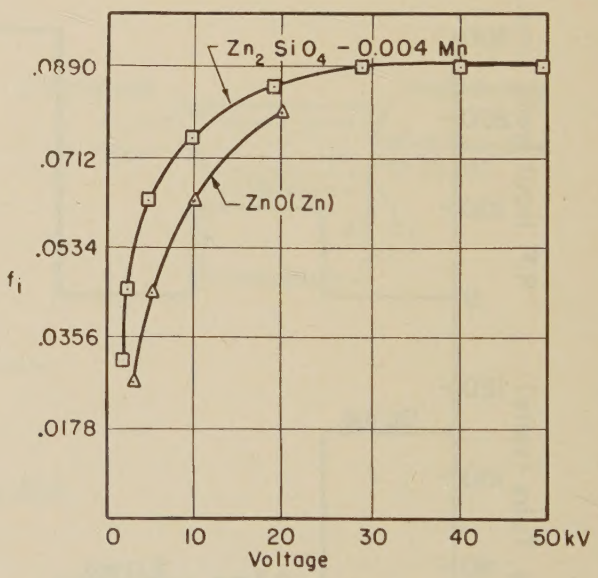


Fig. 3—Absolute efficiencies of two phosphors (after Bril and Klasens).

In order to apply (6) to numerical calculation, it is necessary to express f explicitly as a function of voltage (see Fig. 3).[7,8] It turns out that the function Vf is quite linear with V (see Fig. 4), which means that the function

[7] A. Bril and H. A. Klasens, "Intrinsic efficiencies of phosphors under cathode-ray excitation," *Philips Research Reports*, vol. 7, pp. 401–420; December, 1952.

[8] Data on ZnO(Zn) obtained from Dr. Bril via private communication.

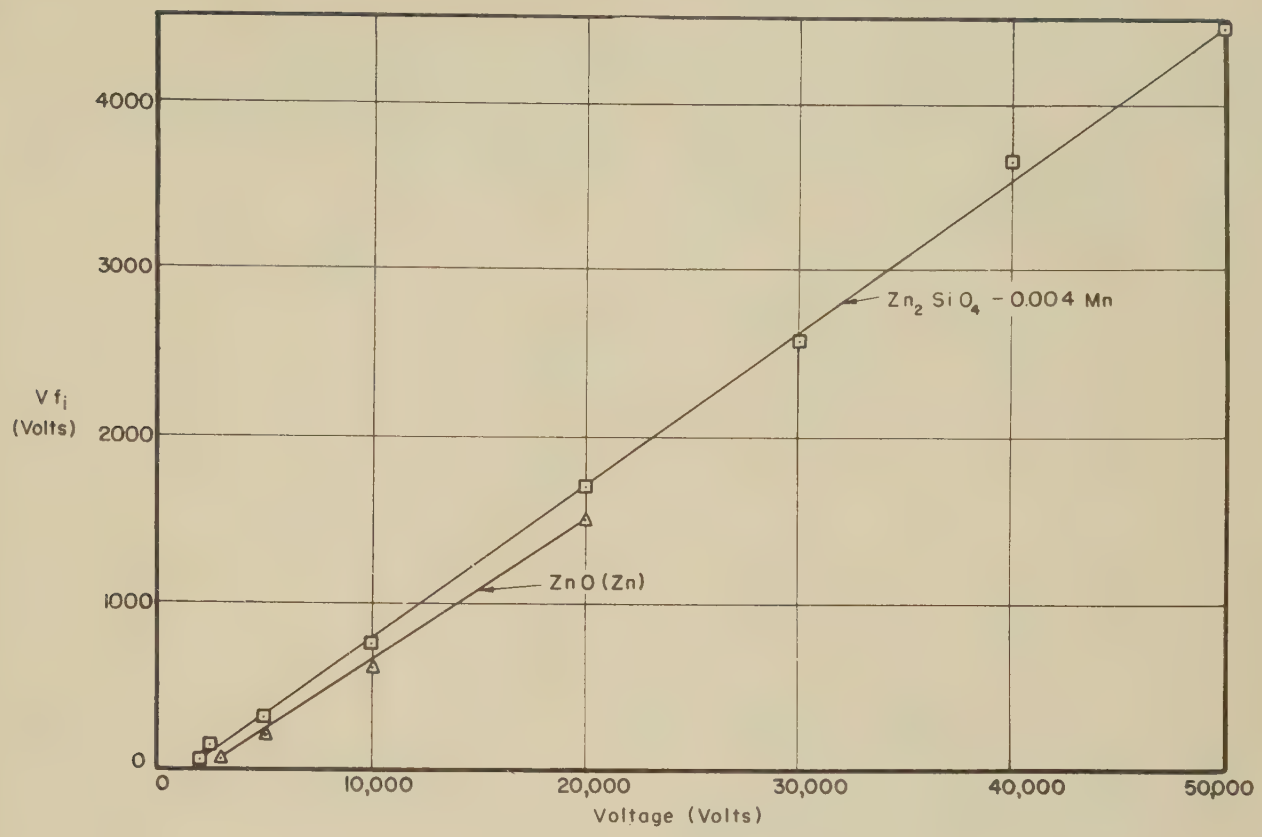


Fig. 4—Hyperbolic law for two phosphors (from the data of Bril and Klasens).

f vs V is a hyperbola of the form $(V-a)(f-b)=-c$, where $a=0$. This reduces to

$$Vf = bV - c \tag{7}$$

where

$$Vf = .0913V - 115 \text{ for the P1 phosphor}$$

and

$$Vf = .085V - 200 \text{ for the P15 phosphor.}$$

This may be used directly in (6) but it is instructive to transpose constants as follows. Since

$$f = b - \frac{c}{V} \tag{8}$$

it is apparent that $b=\lim_{V\to\infty} f$, which we shall call f_∞. Then, if we let $f=0$, $V=V_0=c/f_\infty$. Thus (7) becomes

$$Vf = f_\infty(V - V_0) \tag{9}$$

where V_0 is the appearance potential for the phosphor, provided the hyperbolic law holds at low voltages.

The term Vf that appears in (6) may now be replaced by the right side of (9) to give a usable criterion for feedback equilibrium:

$$2.3t_p t_e f_\infty S_{\max}(V - V_0)M = 1 \tag{10}$$

The single arbitrary variable left for a given tube is V. There is, therefore, a unique value which we shall call V_e, the equilibrium voltage, which just satisfies (10). If we solve for this:

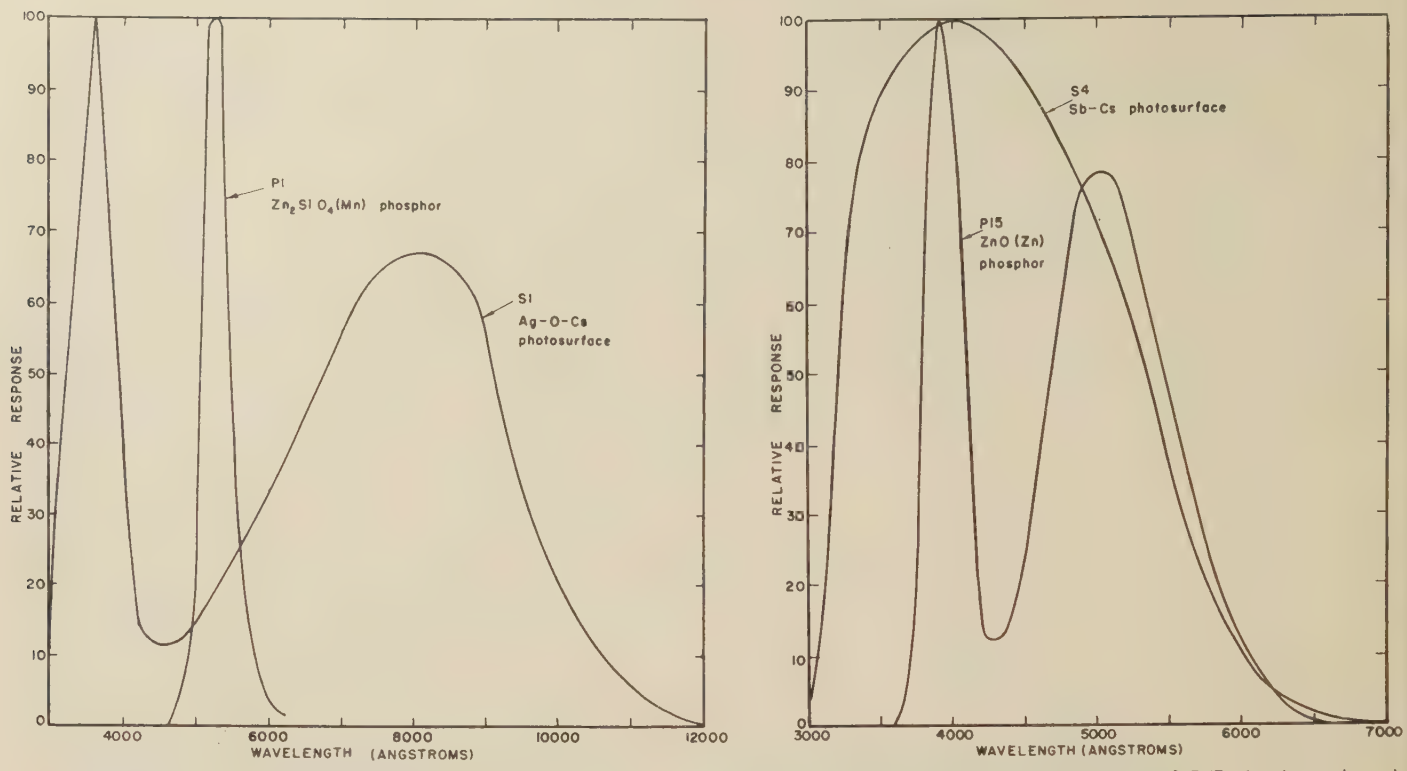
$$V_e = \frac{1}{2.3t_p t_e f_\infty S_{\max} M} + V_0 \tag{11}$$

we finally arrive at an expression giving the characteristic equilibrium voltage for any vacuum diode containing a cathodoluminescent anode and a photosensitive cathode.

A Numerical Comparison of Electrode Pairs

The P1-S1 electrode pair was initially chosen for experimentation because it reputedly involved the least amount of experimental difficulties. This choice later appeared to be a very unfortunate one due to the extreme mismatch between the P1 output and the S1 response. A short inspection of the properties of commercially available materials showed that the zinc oxide, zinc activated phosphor was not only an extremely good match for the antimony-cesium photosurface (R.T.M.A. designations P15 and S4 respectively), but that it was several orders of magnitude faster, too.[9] The relative degree of matching is graphically depicted in Fig. 5. The criterion for feedback equilibrium will be applied to the above two electrode pairs in order to allow a quantitative comparison.

[9] The phosphor response being the rate controlling step, we may compare a decay time of about 3 milliseconds for P1 with 1.5 microseconds for the longwave peak of P15 (.05 microsecond for the ultraviolet peak).



(a) Individual output and response curves for P1 phosphoranode and S1 photocathode

(b) Individual output and response curves of P-15 phosphoranode and S4 photocathode.

Fig. 5—Spectral characteristics of two electrode pairs (data are average values taken from RCA Tube Manual).

In the case of a vacuum photodiode, t_e is assumed to be unity due to the accelerating field. As far as t_p is concerned, we may take tube geometry to be that of a cylinder 9 cm. long and 2.5 cm. in diameter, to which we apply a Lambertian light distribution. An approximate calculation yields a value of .02 which we may expect to be increased to one tenth by reflection of light from the tube walls. The integrals in (5) were computed graphically after selecting and tabulating a sufficient number of points from the L vs λ, and R vs λ curves given in the RCA Tube Handbook. The numerical calculations are summarized in Table I.

Considering the much higher relative matching between electrodes in the P15–S4 pair, as can be seen in Table I and Fig. 5, it is surprising at first to note that V_e for P15-S4 is greater than that for P1-S1. However, since V_0(P15) is considerably greater than V_0(P1), this becomes clear when it is seen that under optimum feedback conditions, (11) approaches $V_e = V_0$. That this situation can actually be achieved is notably apparent in the case of the P15-S4 pair (see Table I).

TABLE I

Equilibrium Voltages for Two Electrode Pairs

	P1-S1	P15-S4	Dimensions
Maximum cathode sensitivity (S_{max}), at the wavelength (λ)	.002 at 8000	.042 at 4000	u-amp/u-watt Å
Maximum intrinsic efficiency (f_∞)	.0913	.085	—
Phosphor appearance potential (V_0)	1260	2360	V
Photon transit efficiency (t_p)	0.1	0.1	—
The integrals:			
$\int_{\lambda_1}^{\lambda_2} L\lambda d\lambda$	2.56×10^6	5.38×10^6	Å²
$\int_{\lambda_3}^{\lambda_4} Ld\lambda$	497	1160	Å
$\int_{\lambda_1}^{\lambda_2} LRd \log \lambda$	0.0109	0.0782	—
The matching constant (M)	56	362	Å
Equilibrium voltage (Ve)	1685	2363	V

Some Notes on Tube Fabrication

The details of construction of the bistable vacuum photodiode have already been described fully.[3] A prime consideration in the construction of the tube was the problem of protecting the phosphor from attack by the cesium vapor during the formation of the photocathode. This was done by covering the phosphor screen with a deep layer of acid washed, ignited silica sand prior to mounting the tube and its appendage containing the cesium source (a Si-Cs_2CrO_4 "getter" filament) on the vacuum manifold. After the tube was evacuated and baked at 450°C overnight, the getter was flashed and the cathode brought to maximum sensitivity. The tube and its appendage was sealed off from the manifold and the sand poured into the getter appendage, after which the latter was sealed off from the tube.

During construction, it would have been highly advisable to include, as a second appendage, an ionization gauge with the tube-getter appendage assembly. In this way it would have been possible to obtain a higher terminal vacuum in the tube by employing the pumping action of the gauge[10] immediately before final seal-off.

Discussion

The similarity in behavior of the present tube and the gas diode glow tube is remarkably complete. The initiating pulse in either case is electromagnetic radiation: $2\frac{1}{2}$ electron volts (optical frequency) in the former case, and about 10^{-8} electron volt in the latter. The forms taken by the curves in Figs. 1 and 2 are obvious counterparts of each other. By drawing a hypothetical load line on part *a* of either Fig. 1 or 2, it is possible to construct the *b* part by moving along the load line as the conditions of "illumination" require. Restricting our attention to Fig. 2 for the sake of clarity we see that pulse number 1 corresponds to the 110 volt point on the abscissa of the conduction curve coordinates. Pulse 2 consists of a burst of two megacycle radio-frequency energy at 100 volts. During this time, the tube must conduct at the intersection of the load line and the 100 volt rf curve. Notice that this point is above the minimum sustaining voltage. During pulse 3, the rf voltage is removed, and the conducting point moves up in voltage and down in current along the load line to the storing curve. The fourth pulse of 300 volts rf causes a relatively heavy current to flow at a tube voltage considerably below sustaining, and when this is removed to go to the fifth pulse, the capacitor in parallel with the load resistor holds the voltage near this point until the current has dropped to a negligible value, and the tube will revert to its initial state. This scheme of operation is equally general for the bistable vacuum diode; to turn the tube on, it is only necessary that the load line intersect the illumination curve at a voltage $V_1 > V_e$, while to turn the tube off the load line and "illumination" curve must meet at a voltage $V_0 < V_e$.

Another consequence of this similarity is that both tubes embody the principles of voltage regulation, the regulating voltage for the photodiode being the V_e of (12). The marked absence of the unique V_e that is obvious in Fig. 1 is presumed to arise out of two sources: (a) the tube was crudely constructed and probably suffered from excessive residual gassiness, with consequent positive ion bombardment of the cathode, and (b) the conduction curves for the vacuum diode shown in Fig. 1 were taken without the load resistor necessary to absorb the excess voltage. The resulting destructive effects would also account for the rapid worsening of the voltage regulating characteristic; the dotted storage curve in Fig. 1(a) was taken a mere three days before the solid one.

[10] D. Alpert, "New developments in *ne* production and measurement of ultra high vacuum," *Jour. Appl. Phys.*, vol. 24, pp. 860–876; July, 1953.

In view of the generic relationship between the present tube and an ordinary image converter tube, one is led to consider the possibility of achieving image storage, with particular reference to the storage of an n^2 array of binary digits. Although the use of internal optical lenses is ruled out completely, it is conceivable that image retention may actually be possible without optical focusing provided the interelectrode spacing is sufficiently reduced, and the electron beam is well collimated. In such a device, it would be possible to add digital information at random, but erasure would have to be an all or none affair. However, if either the anode or the cathode was formed as a mosaic, each unit of which possessed its own RC net, then a truly bistable, random access tube, storing n^2 bits of information would result.

The criterion for bistability, in addition to describing the conditions for feedback equilibrium, also contains the restriction on the self-triggering of the tube, either by thermionic emission from the cathode, or cosmic ray excitation of either electrode. Such self-excitation is undoubtedly present, but it does not appear likely that either type could cause triggering. Thermionic emission, the source of the ordinary dark current in a phototube consists of a constant, very low level of current passing from cathode to anode. Now, the logic on which the general criterion is based states that, provided there is present initially a current that tends to increase without limit, except for the effects of voltage drops so engendered on the efficiency of the phosphoranode, equilibrium will be established (see the discussion following equation 2). If the current is less than this value, the feedback must decay to zero. Thus the dark current in the present type of tube will do no more than it does in an ordinary photodiode.

The case of cosmic ray triggering corresponds to an accidental, high intensity, short duration effect that might turn the tube on. Inasmuch as equilibrium conditions in the single tube constructed so far produced a visible glow on the anode, accompanied by a fairly heavy photocurrent, one concludes that this type of triggering must start either with a scintillation of light from the anode or a burst of electrons from the cathode. Of course, this could not be observed as such in a tube possessing feedback. But, if this were so, it should be possible to observe random scintillation on an ordinary cathode ray tube screen with only the high voltage and focusing coils on, or random surges of current in an ordinary darkened photodiode with the accelerating potential on.

Finally, it certainly should be possible to derive from (2), an appropriate expression for a solid state electro-optical storage device consisting of an electroluminescent screen and a photoconductor, although the situation would be complicated by the nonlinear dependence of the resistance of the photoconductor on illumination.

With regard to the introduction of an explicit function for phosphor efficiency, Bril and Klasens did their work

on infinitely thick layers, which they found to correspond to screen densities of 20 milligrams per square centimeter or greater. Screen densities in the present work were about 6 milligrams per square centimeter, and were bound to the substrate with potassium silicate. Bril and Klasens do not mention the use of a binder. One would naturally expect a binder of any sort to decrease the efficiency of a phosphor. Furthermore, according to the above authors, a screen density of 6 milligrams per square centimeter corresponds to maximum light emission on the glass side of the phosphor screen: the "wrong" side in this case. These facts seem to militate in favor of very dense screens, but recent work[11,12] on ZnO(Zn) screens indicates that extremely thin, "monoparticle" screens, deposited with no binder at all, on a conductive backing may be highly efficient since they have been observed to emit visible light at accelerating potentials as low as 3 volts. The conductive backing could very easily be a highly reflecting metal film in order to enhance further the gun side emission.

It is obvious that the values of V_e given in Table I are very much dependent on V_0. A private communication from Dr. Bril has indicated that the hyperbolic law for phosphor emission breaks down at very low voltage so that the true appearance potential may be considerably lower than V_0. Thus there is no essential contradiction between the findings of Kaisel, Clark, and Shrader and those of Bril and Klasens for the ZnO(Zn) phosphor nor between the experimentally determined V_e of 800 volts for the P1-S1 electrode pair shown in Fig. 1 and the predicted value of 1685 volts from Table I. Regardless of the true value of V_0, a favorable V_e should be obtained when the fraction in (11) is minimized (compare 425 volts for the P1-S1 pair with 3 volts for the P15-S4 pair).

ACKNOWLEDGMENT

The author would like to extend his appreciation to Dr. Fred A. Schwertz and Dr. John R. Bowman for their generous assistance and encouragement in this work.

[11] S. F. Kaisel and C. B. Clark, "A luminescent screen for use with very low velocity electrons," *J. Opt. Soc. Am.*, vol. 44, pp. 134–135; February, 1954.
[12] R. E. Shrader and S. F. Kaisel, "Excitation of zinc oxide phosphors by low energy electrons," *J. Opt. Soc. Am.*, vol. 44, pp. 135–139; February, 1954.

Ternary Counters*

R. S. MACKAY† AND R. MACINTYRE‡

Summary—**Counter stages having three stable states, and using no more components than standard binary counters, have been built by properly using the already present nonlinearity of grid current. Problems of stability, cascading, and decoding have been worked out.**

INTRODUCTION

BINARY COUNTERS generally use fewer tubes to reach a given count than any of the other commonly used circuits. However, if a counter could be made having a number of tubes and other components comparable with a bistable unit, and yet have more stable states (a higher number base), then one could go to higher counts with considerably fewer components. There follows an approach to the problem.

A bistable multivibrator can be given a third intermediate stable state if, during a transition, some nonlinearity is used to load suddenly the circuit and reduce its loop gain below unity. The switching process will then stop, and another pulse will be required to knock the circuit from this middle state and carry it on to the end state. In essence, the present circuits accomplish this by allowing both grids to draw current part way through a transition; thus each gives a low impedance for the other tube to work into and the over-all gain is reduced (the feedback amplifier is partially "shorted"). The circuit must fall into this middle state when progressing in one direction but must miss it when going in the other if it is to count or scale in the ternary system. A suitably asymmetric condenser placement provides a transient switching memory (which is quite independent of the steady state condition of tristability) that forces the circuit to cycle through the states in the manner that a counter must. The resulting circuits are stable over an acceptable range of voltages and pulse sizes.

With most tube types, if the grid current nonlinearity is not augmented, one must restrict the maximum loop gain in the circuit in order to assure the existence of the third or central state. This will limit the transition speed and thus one generally finds, in practice, that these circuits are not the very fastest. For a similar reason these circuits, during all transitions, readily display

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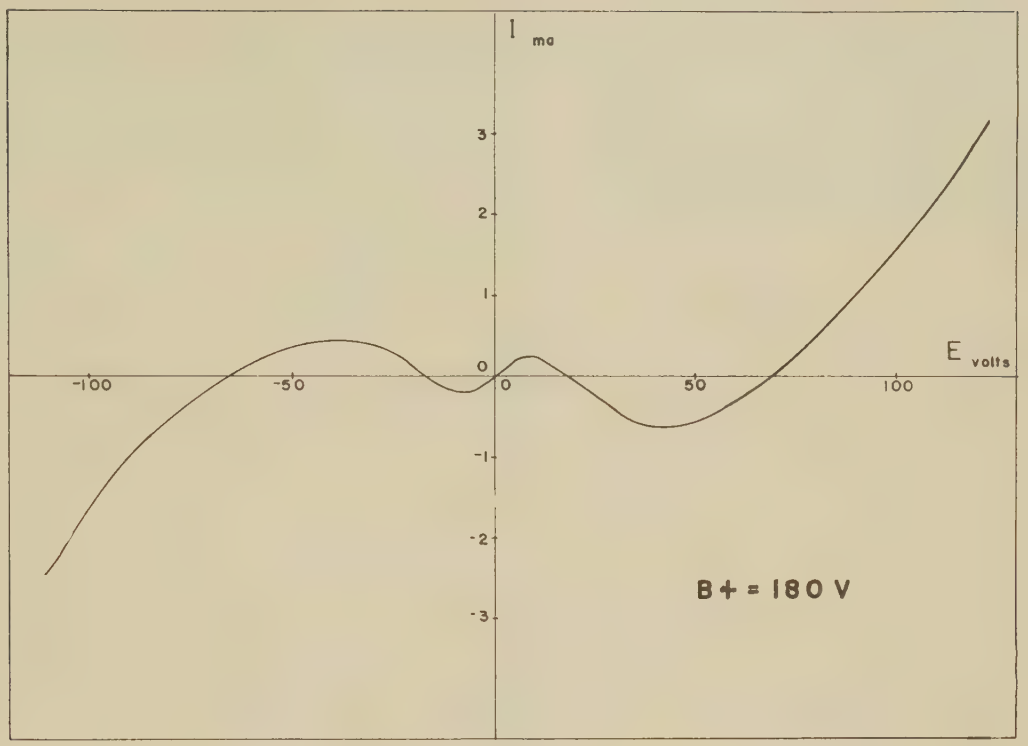

Fig. 1—Double negative resistance characteristic of tristable circuits. The symmetry of this graph suggests good stability against disturbances.

ıe "perching" characteristic of two-state devices.[1] It ight be noted that a study of these circuits is pedagogi-lly excellent because it makes more definite some of ıe concepts involved in common bistable circuits.

This type of operation can sometimes be observed ccidentally in binary circuits because of the capacity the oscilloscope probe, though the circuit may go ack to counting by two rather than three when not eing observed.[2,3] Another method that has been used achieve tristability is to add extra nonlinearity in the rm of diodes that change the loop gain by coupling ıd decoupling cathode resistors.[4] In this case, a fairly ɔmplicated transient switching memory was provided allow counting action.

Bistable electric devices are characterized by an ectrical negative resistance, and their switching con-sts of transitions between the two surrounding regions positive slope; *i.e.*, between the two intersections of a ad line and the positive incremental resistance regions. tristable device should have two negative slope re-ons separating three positive slope regions. If one ots current as a function of a voltage applied from ate to plate in one of these modified multivibrators ıen one obtains the curve of Fig. 1. The two inter-

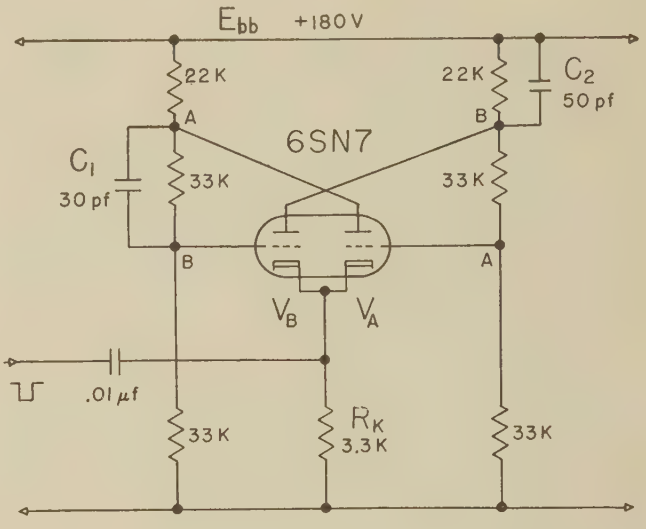

Fig. 2—Basic ternary counter circuit.

sections of the horizontal axis with the negative sloping parts of the curve correspond to unstable conditions. In a mechanical analog they would be the crest of two mountain peaks around which were three valleys, and over which a ball is rolling; the ball can stop in any valley but will not long balance on a peak.[1]

Tristable Counter

An example of a ternary counter is shown in Fig. 2. The circuit is similar to that of a bistable counter except R_k is proportionately lower in resistance and one of the capacitors is connected to $B+$ (ac ground) instead of being used in the cross-coupling position. The three

[1] R. S. Mackay, "Switching in bistable circuits," *Jour. Appl. ys.*, vol. 25, p. 428; 1954.
[2] A. D. Booth and J. Ringrose, "A three state flip-flop," *Elect. ıg.*, vol. 23, p. 133; April, 1951.
[3] K. C. Johnson, "A three state flip-flop," *Elect. Eng.*, vol. 23, p. 7; June, 1951.
[4] R. Weissman, "High speed counter using ternary notation," *ectronics*, vol. 25, p. 118; 1952.

stable states are indicated by the plate A waveform, Fig. 3, and are defined below. (Plate B cycles between the same three states in the reverse manner, cf. Fig. 7.)

0 state, V_B cutoff, V_A on and drawing grid current.
1 state, V_A and V_B on and drawing grid current.
2 state, V_A cutoff and V_B on and drawing grid current.

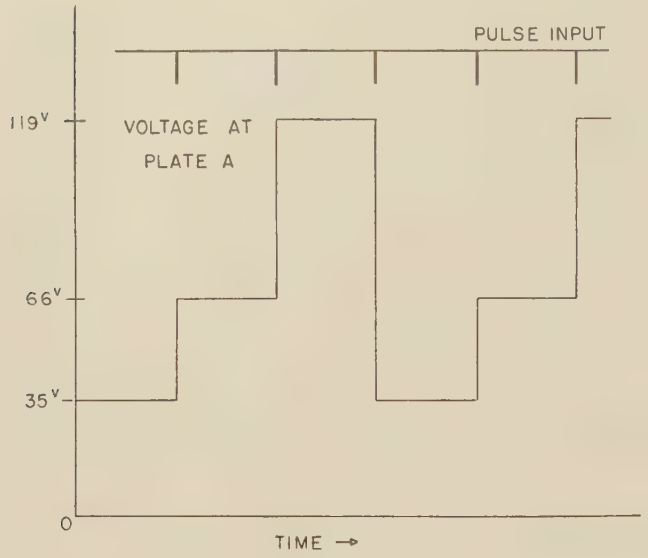

Fig. 3—Plate A waveform.

The transitions are termed "0-1" for a transistion from the 0 state to the 1 state, "1-2" for a transition from the 1 state to the 2 state and "2-0" for a transition from the 2 state to the 0 state. To simplify the discussion, it will be assumed that the impedance of a conducting grid is small compared to 22K ohms. The beginning of the input pulse to the 6SN7 cathode will be termed the "negative step" and will occur at time t_1. The end of the pulse will be termed the "positive step" and will occur at time t_2.

At time t_2^+ (just after t_2) for any transition the circuit voltages will be a set of values such that the circuit will be in one of the three stable states and when the circuit is left in this condition, it will seek the equilibrium values for that state.

The voltages for the ternary counter are shown in Table I below.

TABLE I

V_A			V_B		State
Plate	Grid	Cathode	Plate	Grid	
35v	28.7v	25.7v	119v	17.7v	0
66	28.8	28.5	66	28.8	1
119	17.7	25.7	35	28.7	2

These values are for an average 6SN7. The cathode voltage, for only one tube conducting, will be about 26 volts. If it is assumed that grid current starts to flow at $E_{gk}=0$, then grid current will flow in grid A when $E_{pB}=2\times26$ v $=52$ v. If grid current flows in both grids, the cathode voltage will rise to about 28 volts, so $E_{pB}=2\times28$ v $=56$ volts. Therefore, in the region of $E_p=52$ to 56 volts, grid current will flow and will effectively connect the 30 pf condenser and 33K from one side of the circuit and the 33K resistor on the other side of the circuit to the cathode. This causes the product of the gains, $G_A \cdot G_B$, to be less than unity. (Actually the dc gain is higher than the ac gain but it also must be less than unity for stability.) This condition defines the 1 state.

The 0 state and 2 state are similar to the two stable states of the binary type of circuit. While grid current in the "on tube" is not necessary for the 0 state and 2 state of the ternary circuit, it will contribute to stability due to the plate loading.

The Transitions of the Ternary Counter

Fig. 4 is a record of the transitions between the various states. The input pulse had a duration of 1 μs and an amplitude of about 22v. The input pulse, which is transferred to the grids in all of the transitions, is clearly distinguishable in all of the grid waveforms. Note that the grid waveforms are not shown in the same scale as the plate waveforms. The transfer of the input pulse to plate A is indicated by the straight, vertical segments of each of the plate A waveforms.

In the top row of the waveforms, all three transitions are superimposed. The dots in each of the waveforms indicate the three voltage levels.

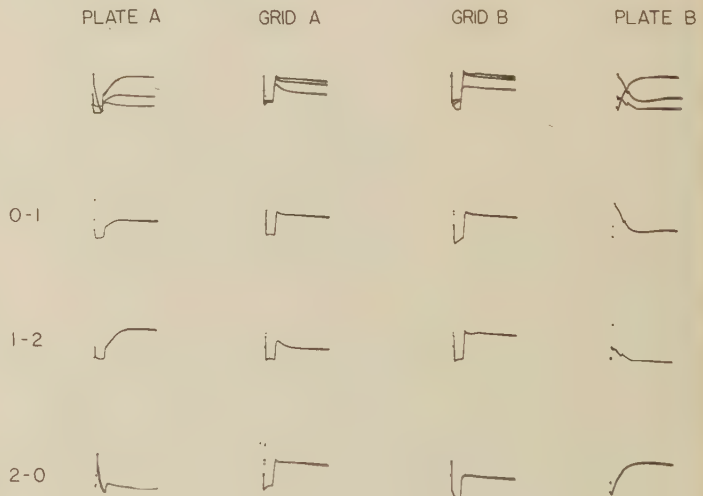

Fig. 4—Ternary counter transition for an input pulse of 1 μs duration and amplitude of 22v. The grid waveforms were given approximately three times the amplification of the plate waveforms in order to show the detail more clearly.

Transition 0-1

In switching from the 0 state to the 1 state, the t_1^- (just before t_1) condition is grid A conducting, grid B cutoff. The negative input step at time t_1 causes a negative step to appear at grid A and at plate A. The negative step is transferred to plate A by means of the R_p

f V_A. Due to the 30 pf, the negative step will also appear at grid B. Hence V_B will still be cut off. The negative voltage step at grid A will cause the 50 pf condenser o begin to charge and therefore the voltage at plate B ill begin to decrease exponentially. Also, the 30 pf ondenser will begin to discharge, raising the grid B oltage slightly, and V_B will start conduction, causing he voltage at plate B to begin to decrease more rapidly. he positive step at t_2 will appear at grid A (since the oltage at plate B has not decreased enough to cause rid A to be cut off by the step) at plate A and at grid B. his action will cause grid B to start conduction. Hence oth grids are conducting and the requirements for the state are satisfied.

ransistion 1-2

The t_1^- condition is both grids conducting. The negative step at t_1 will appear at both grids and at plate A ue to the R_p of V_A and grid B conduction. Consequently the grid A voltage will not change very much between and t_2. Because of the 50 pf condenser from plate B o ac ground, the negative step will not appear at late B, but the voltage of plate B will begin to decrease nd by t_2 it will be low enough so that grid A will be utoff by the positive step. Because grid B is conducting uring the positive step, it will transfer the step to late A, through the 30 $\mu\mu$f. This leaves grid B conducting, grid A cut off and hence the requirements of the state are satisfied.

ransition 2-0

The t_1^- condition is grid B conducting and grid A utoff. At t_1 the negative step appears at grid A, reuced by E_{gk}, due to grid A conduction after the negative step reaches the grid A bias value of E_{gk}. Conduction in grid B causes a large negative step in its voltage hich is transferred to plate A by the 30 pf condenser. fter this initial step, the plate A voltage will continue o decrease, but at a slower rate. Grid B is cutoff by this ction and plate B will start to rise towards its maximum alue. This causes grid A to be left on after the positive tep. A positive step appears at plate A because of this, ut it is not enough to bring grid B back into conduction. ence grid A is conducting and grid B is cutoff which is he requirement for the 0 state.

Permissible Variation of Input Pulse Height

For the circuit of Fig. 2, the transition 0-1 limits the ariation in pulse height for proper operation. Too large pulse will cause the circuit to "overshoot" the middle tate and there will be only two useful states for counting. In this case the waveform, plate B, 0-1, will fall too ar, causing grid A to turn off after time t_2.

Too small a pulse will not drive the circuit out of the state, due to the fact that grid B is not left on at the nd of the input pulse. Fig. 5 shows the permissible ariation of the input pulse for a range of $B+$ voltages from +120v to +240v, for a typical 6SN7. Variations from these values are not more than ±10 per cent for most 6SN7's. The max-min curves for a slightly larger cathode resistor are also shown. The values of $E_{bb}=180$v and $R_k=3.3$K were chosen as a compromise. A smaller E_{bb} causes a smaller variation in plate voltage swings; larger cathode resistor requires a larger input voltage.

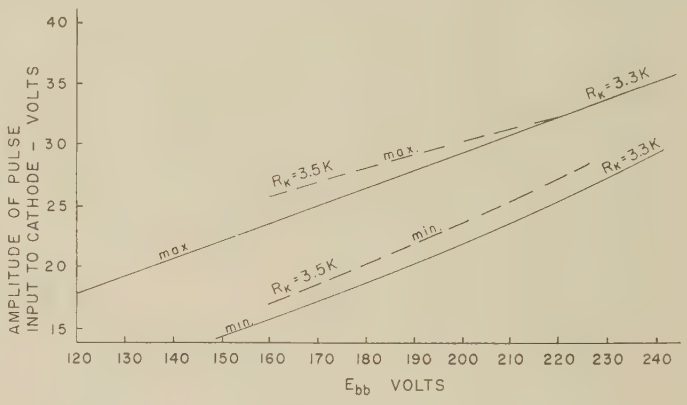

Fig. 5—Max-min amplitude limits of 1 μs negative input pulse for ternary counter operation for a range of $B+$ voltages.

Cascading Ternary Counters

Because of the sensitivity of ternary counter operation to pulse length and height, it appears that the best method of cascading the counters is to use a common pulse line connected to each counter by means of a pulse gate. The relatively low input impedance and high output impedance of the ternary counter suggests a cathode follower type pulse gate. Since the control input to such pulse gates is in the form of a voltage level which can either permit the pulse to pass or not pass, only two levels from the ternary counter can be utilized for a particular gate control input. Since the pulse gate is of the low pass type (*i.e.*, will pass the pulse when the control voltage is at the lower of its two values), a choice of using two of the ternary counter output levels for the pass condition and one for the stop condition or one level for the pass condition and two for the stop condition is possible. The latter case was chosen for the circuit of Fig. 6. In this circuit the maximum voltage applied to the control grid is clamped to +65v by a diode, because otherwise the cathode of the gate tube would rise above +65v when the preceding counter switched to the 0 state, which would cause a positive pulse to appear at the cathode of the following counter. The .47M resistor was chosen because a delay of at least 1 μsec must occur so that the pulse being passed by the gate is not cut short, or the latter part of a pulse permitted to pass.

A timing diagram for the circuit of Fig. 6 is shown in Fig. 7. Note that the pulse input to G_3 is from the output of G_2. An alternative to this would be to mix the levels from T_{1B} and T_{2B} by means of a diode mixer and then apply it to the control grid of G_3. The pulse input for the gate would then be supplied by the pulse line.

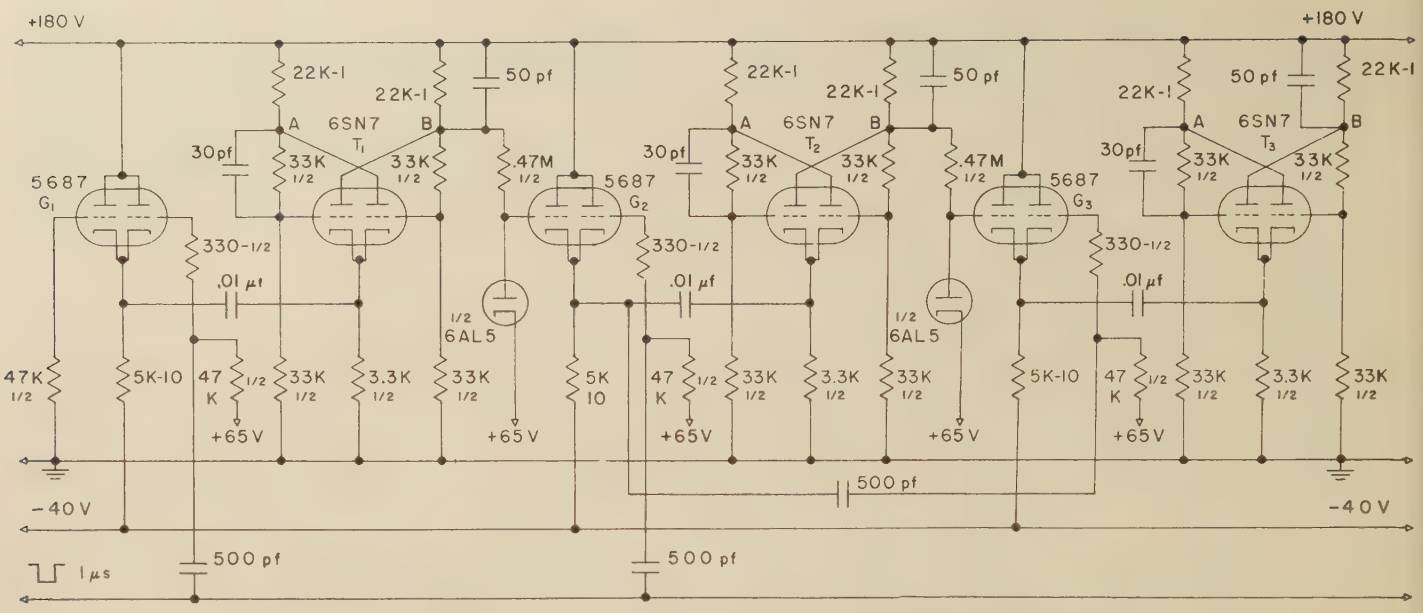

Fig. 6—Cascaded ternary counters using cathode follower type pulse gates.

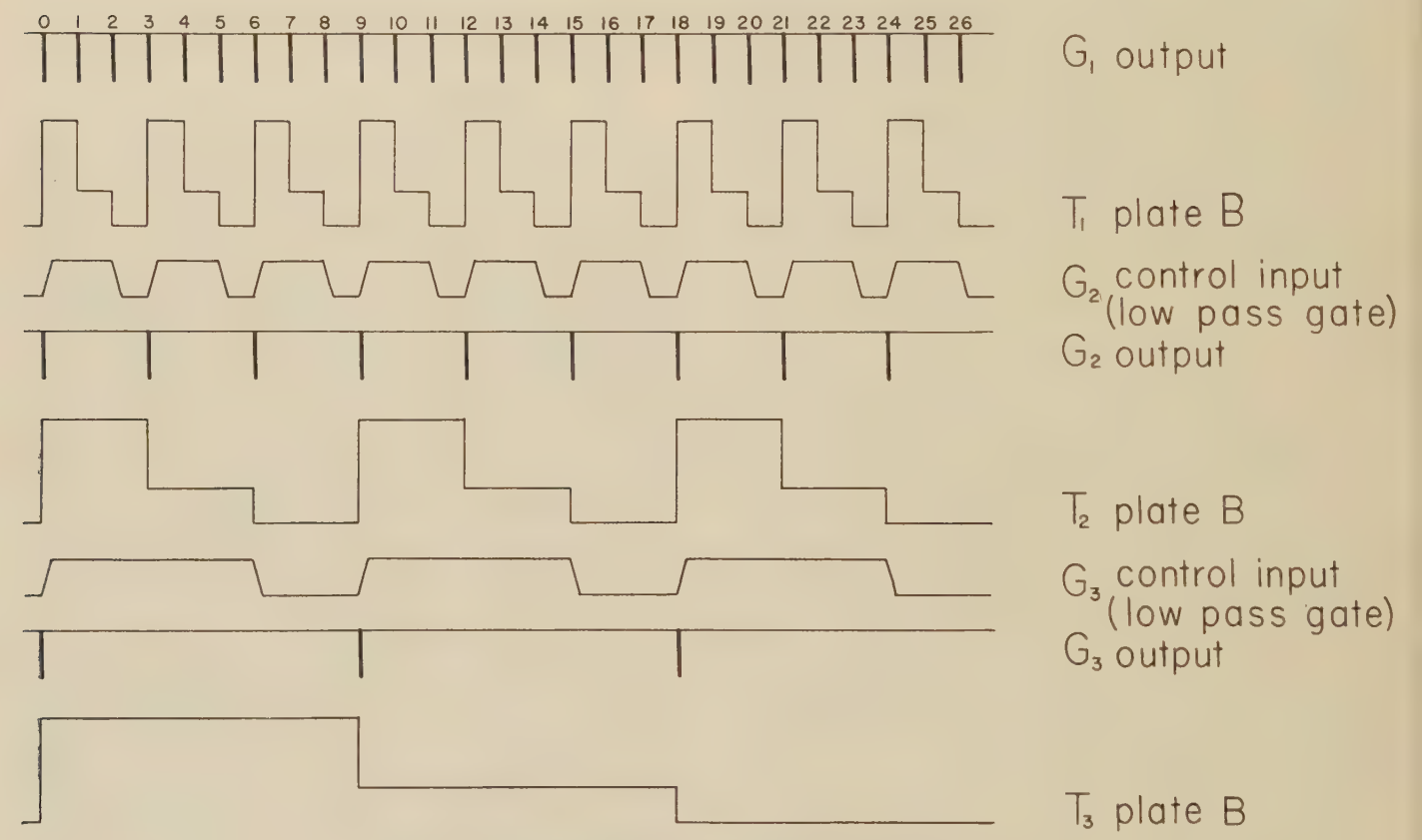

Fig. 7—Timing diagram for the cascaded ternary counters of Fig. 6.

This would result in a better pulse shape for T_3 at the expense of a few more components. G_1 is left in the pass condition for all input pulses in the circuit illustrated. G_1 was included for two reasons. First, since the amplitude of the input pulse is reduced slightly in "passing through" the gate, the pulse heights applied to the counter cathodes will be more uniform as none of them will be applied directly to a counter. Note that the pulse applied to the T_3 cathode is reduced twice. Second, it provides a means of applying an external control to the first counter.

From timing diagram of Fig. 7, it is seen that G_1 divides number of input pulses by one, G_2 divides by three and G_3 by 9. A low-pass gate, whose control level was formed by mixing control levels formed by T_1, T_2, and T_3 would divide number of input pulses by 27.

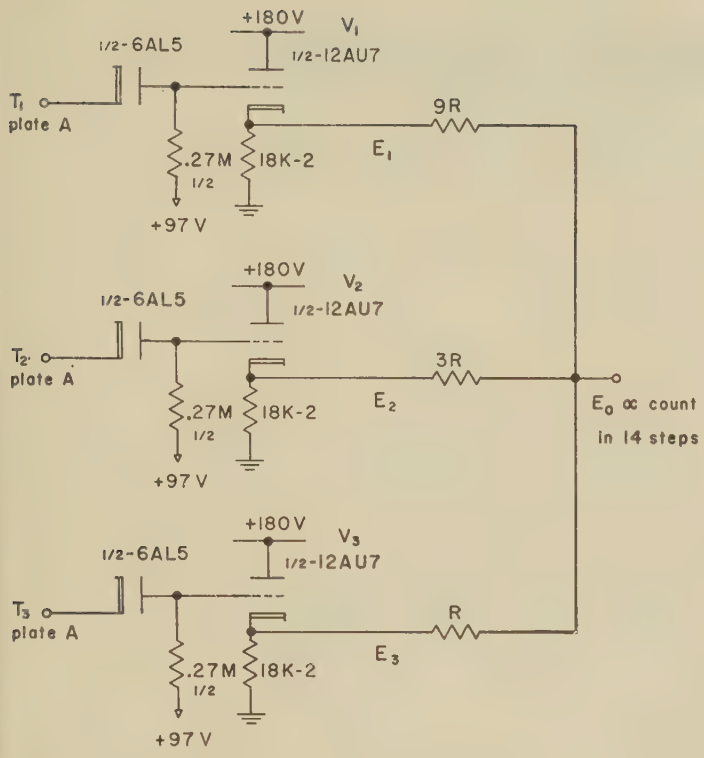

Fig. 8—Ternary count read-out circuit. The three ternary resistors alone would be sufficient if the voltage steps at the plate were both equal.

An alternative system of grid input instead of cathode input was attempted with the ternary circuit of Fig. 2. The proposed method was to use crystal diode pulse gates, to grids, which were controlled by plate voltages. Method worked but was not reliable. Investigation of this mode of operation was not pursued further.

A method of reading out the count on the circuit in Fig. 6 is shown in Fig. 8. Here $E_0=1/13(E_1+3E_2+9E_3)$ where E_1, E_2 and E_3 are the voltages of cathode followers V_1, V_2 and V_3, respectively. E_1, E_2 and E_3 can assume any one of three values E_A, E_B and E_C where $E_A-E_B=E_B-E_C$ and $E_A>E_B>E_C$. If T_1, T_2 and T_3 are counters with the values indicated in Fig. 1, E_A, E_B and E_C will be approximately equal to 98v, 72v, and 46v, respectively. Then $E_A-E_B=E_B-E_C=26$v. Now, for example, after pulse number "0" has occurred (see Fig. 7) the count will be "0 0 0," that is, plate A of each of the counters will be at the lowest of its three possible levels and the outputs of the cathode followers V_1, V_2, V_3 will all be at 46 volts (assuming that the output impedance of a counter is small compared with $.27M$). The output voltage, E_0 will then obviously be 46 volts.

After pulse number "1" has occurred, the count will be 1 0 0, that is, plate A of counter T_1 will be at the intermediate of its three possible levels and counters T_2 and T_3 will be the same as before. Then $E_0=1/13$ $(72+3\cdot46+9\cdot46)=48$v. For a count of 2 0 0, $E_0=1/13$ $(98+3\cdot46+9\cdot46)=50$v.

Starting from pulse number "0," then, the count proceeds as in Table II, where E_0 is the output voltage read by a voltmeter with a +46v reference.

TABLE II

Pulse Number	Count	E_0
0	0 0 0	0
1	1 0 0	2
2	2 0 0	4
3	0 1 0	6
4	1 1 0	8
5	2 1 0	10
6	0 2 0	12
7	1 2 0	14
8	2 2 0	16
9	0 0 1	18
10	1 0 1	20
11	2 0 1	22
12	0 1 1	24
13	1 1 1	26
14	2 1 1	28
15	0 2 1	30
16	1 2 1	32
17	2 2 1	34
18	0 0 2	36
19	1 0 2	38
20	2 0 2	40
21	0 1 2	42
22	1 1 2	44
23	2 1 2	46
24	0 2 2	48
25	1 2 2	50
26	2 2 2	52

In the count indicating circuits, the diodes and $0.27M$ resistors which are connected to +97v are used to obtain equal voltage steps, that is, to satisfy the condition $E_A-E_B=E_B-E_C$. This arrangement, together with the cathode followers, was chosen only to illustrate a method of applying E_1, E_2 and E_3 to the resistors R, $3R$ and $9R$ and does not necessarily represent the best method for accomplishing this. Note that R is considered large with respect to the cathode impedance of the cathode follower.

A 6J6 was substituted for the 6SN7 in the basic ternary counter circuit, Fig. 2. The circuit operation was satisfactory. However, a lower amplitude pulse was required at the cathode for operation. For E_{bb} =180v, the pulse could vary between 9v–12.5v for most of the 6J6 tubes that were tested.

A Logarithmic Voltage Quantizer*

E. M. GLASER† AND H. BLASBALG†

Summary—This paper describes an analog to digital converter which converts voltage into a number which is proportional to the logarithm of the voltage. The device is completely automatic. It can handle input data at the rate of 10,000 voltage samples per second. The accuracy of conversion or quantization is determined by the designer's selection of the circuit parameters. The Radiation Laboratory quantizer has a maximum quantization error of 5 per cent. Samples of duration greater than .5 microsecond can be quantized.

Introduction

THE CONVERSION of analog data to digital form is most commonly performed in a linear fashion, that is, the digital output is proportional to the analog input. Very little attention has been given to converters which operate nonlinearly on the analog input. One nonlinear analog to digital conversion of some importance is the logarithmic. The direct logarithmic conversion, or quantization, of analog data can be performed quite simply and rapidly without the use of logarithmic attenuators preceding linear quantizers. The method of quantization is as follows:

The quantizer accepts a voltage sample and converts it to an equivalent pulse whose duration is porportional to the logarithm of the voltage of the sample. The pulse duration is quantized linearly by counting the number of pulses produced by a fixed frequency pulse generator during the interval. This number is then proportional to the logarithm of the input sample.

The conversion from voltage to time is performed in a simple RC circuit. The mathematical analysis of the conversion and quantization is given below. From the analysis useful design equations are obtained.

Analysis

An RC network shown in Fig. 1 is charged to voltage E by closing of switch S. After the switch is opened at $t=0$, the voltage $e(t)$ decays exponentially:

$$e(t) = E \exp(-t/RC). \tag{1}$$

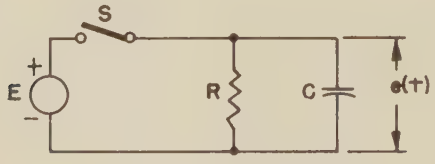

Fig. 1—Exponential decay network.

Let T=time for $e(t)$ to decay to a fixed voltage, E_T. Then,

$$E_T = E \exp(-T/RC) \tag{2}$$

or,

$$E = E_T \exp(T/RC) \tag{3}$$

and,

$$\log E = \log E_T + \frac{T}{RC}. \tag{4}$$

T is therefore a linear function of $\log E$.

T is now subdivided into equal increments ΔT and the number of complete increments required for E to decay to E_T is counted.

Let E_n=value of E which decays to E_T in exactly $n\Delta T$ seconds and E_{n+1}=value of E which decays to E_T in exactly $(n+1)\Delta T$ seconds then,

$$E_0 = E_T.$$

From (4)

$$\log E_n = \log E_T + \frac{n\Delta T}{RC} \tag{5}$$

and,

$$\log E_{n+1} = \log E_T + \frac{(n+1)\Delta T}{RC}. \tag{6}$$

Subtracting (5) from (6),

$$\log E_{n+1} - \log E_n = \frac{\Delta T}{RC} = \frac{\Delta T}{\tau} \tag{7}$$

where

$$\tau = RC.$$

Let,

$$\overline{E_n} = \tfrac{1}{2}(E_{n+1} + E_n)$$

and,

$$\Delta E_n = E_{n+1} - E_n.$$

Then,

$$\frac{\Delta E_n}{\overline{E_n}} = 2\left(\frac{E_{n+1} - E_n}{E_{n+1} + E_n}\right) = 2\left(\frac{E_{n+1}/E_n - 1}{E_{n+1}/E_n + 1}\right). \tag{8}$$

This can be written in exponential form

$$\frac{\Delta E_n}{\overline{E_n}} = 2\left(\frac{\exp(\Delta T/\tau) - 1}{\exp(\Delta T/\tau) + 1}\right) = 2\tanh\frac{\Delta T}{2\tau}. \tag{9}$$

Expanding the right hand side gives

$$\frac{\Delta E_n}{\overline{E_n}} = \frac{\Delta T}{\tau} - \frac{1}{12}\left(\frac{\Delta T}{\tau}\right)^3 + \cdots. \tag{10}$$

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Neglecting all but the first term of the series gives

$$\frac{\Delta E_n}{\overline{E_n}} \approx \frac{\Delta T}{\tau}. \tag{11}$$

The error, δ, in this approximation has an upper limit

$$\delta < \frac{1}{12}\left(\frac{\Delta T}{\tau}\right)^3.$$

Solving (8) for E_{n+1} gives

$$E_{n+1} = E_n\left\{\frac{1+\frac{1}{2}\frac{\Delta E_n}{\overline{E_n}}}{1-\frac{1}{2}\frac{\Delta E_n}{\overline{E_n}}}\right\} = rE_n \tag{12}$$

where

$$r = \frac{1+\frac{1}{2}\frac{\Delta E_n}{\overline{E_n}}}{1-\frac{1}{2}\frac{\Delta E_n}{\overline{E_n}}} \approx \frac{1+\frac{1}{2}\frac{\Delta T}{\tau}}{1-\frac{1}{2}\frac{\Delta T}{\tau}} \tag{13}$$

from (11). Using (12)

$$E_n = r^n E_0 \tag{14}$$

showing that the quantized voltage levels form a geometic series.

The maximum quantization error will occur when either E_n or E_{n+1} is quantized as $\overline{E}_n$. This error, S, will be, in either case

$$S = \text{max. error} = \frac{1}{2}\frac{\Delta E_n}{\overline{E}_n} \approx \frac{1}{2}\frac{\Delta T}{\tau}. \tag{15}$$

If N = maximum number of quantized time intervals, and E_N = maximum quantizable voltage, then the voltage range, R, of the quantizer is

$$R = \frac{E_N}{E_T} = \frac{E_N}{E_0} = r^N \tag{16}$$

$$\log R = N \log r = N \log\left(\frac{1+S}{1-S}\right)$$

$$= 2N\left(S + \frac{1}{3}S^3 + \frac{1}{5}S^5 + \cdots\right). \tag{17}$$

And again, by neglecting all but the first term

$$\log R \approx 2NS \tag{18}$$

with error, γ, given by

$$\gamma < \frac{2}{3}\frac{NS^3}{1-S^2}.$$

Then

$$N \approx \frac{1}{2S}\log R. \tag{19}$$

The rate at which the exponential $e(t)$ decays when $e(t) = E_T$ is

$$\left.\frac{de(t)}{dt}\right|_{t=T} = \frac{-E}{RC}\exp(-T/RC)$$

and from (2)

$$\left.\frac{de(t)}{dt}\right|_{t=T} = \frac{-E_T}{RC} = \frac{-E_T}{\tau}.$$

The rate of voltage decay at the threshold is therefore independent of the initial sample voltage E. The accuracy of the threshold amplitude comparator is therefore constant throughout the quantization range.

The equations useful for quantizer design are given below.

$$\text{max. error} = S = \frac{1}{2}\frac{\Delta T}{\tau}. \tag{15}$$

The number of quantization intervals is given by,

$$N = \frac{1}{2S}\log R. \tag{19}$$

The quantizer used at the Radiation Laboratory was designed to operate with 5 per cent maximum quantization error. The number of quantized levels was chosen to be 32 to permit use of a 5 stage binary register in recording the output count.

With $S = .05$ and $N = 32$ the voltage range is

$$R = \log^{-1} 2NS = 24.5. \tag{20}$$

The quantizer generates a pulse at the end of each ΔT interval following the start of the exponential decay if $E > E_T$. This process continues until the threshold E_T is reached (Fig. 2, next page).

Voltage	No. of Pulses
$E_T \leqq E < rE_T$	0
$rE_T \leqq E < r^2E_T$	1
$r^2E_T \leqq E < r^3E_T$	2
. . . . .	. . .
$r^{N-1}E_T \leqq E < r^NE_T$	$N-1$
$r^NE_T \leqq E$	N

For $R = 24.5$, $S = .05$ the maximum number of pulses generated is $N = 31$.

The time increment of quantization is one μsec. This minimizes analysis time without unduly complicating the device. The time constant is determined from (15). For $s = 0.05$

$$\tau = \frac{\Delta T}{2S} = \frac{1 \times 10^{-6}}{2 \times .05}$$

$$\tau = 10 \times 10^{-6} \text{ sec.}$$

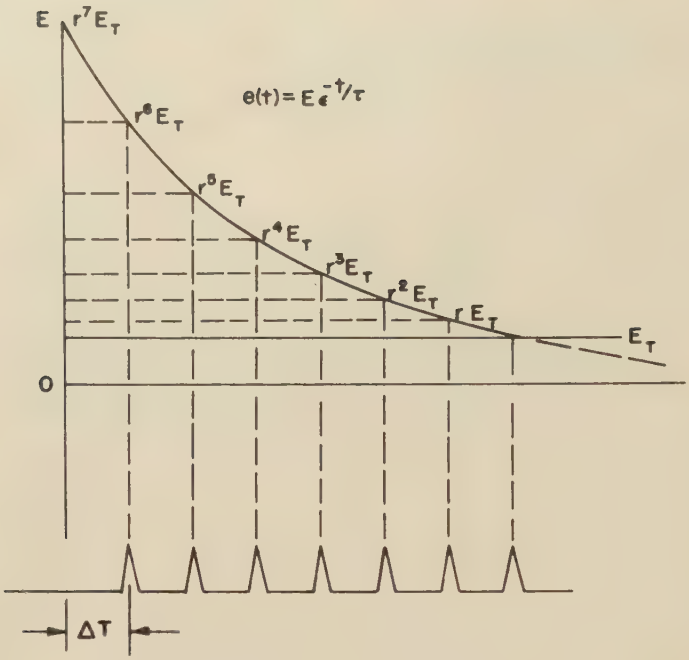

Fig. 2—Quantized exponential decay.

A table relating input voltage to $\overline{E}_n$ and the quantization level (number of output pulses +1) is shown in Fig. 3 for $S=.05$.

S=.05 (5% QUANT.)		
INPUT VOLTAGE	QUANT. LEVEL	$\overline{E}_n$
3.00 – 3.32	1	3.16
3.32 – 3.66	2	3.49
3.66 – 4.05	3	3.86
4.05 – 4.48	4	4.26
4.48 – 4.95	5	4.71
4.95 – 5.47	6	5.21
5.47 – 6.04	7	5.75
6.04 – 6.68	8	6.36
6.68 – 738	9	7.03
7.38 – 8.15	10	7.76
8.15 – 9.01	11	8.58
9.01 – 9.96	12	9.43
9.96 – 11.0	13	10.5
11.0 – 12.2	14	11.6
12.2 – 13.4	15	12.8
13.4 – 14.9	16	14.1
14.9 – 16.4	17	15.6
16.4 – 18.2	18	17.3
18.2 – 20.1	19	19.1
20.1 – 22.2	20	21.1
22.2 – 24.5	21	23.3
24.5 – 27.1	22	25.8
27.1 – 29.9	23	28.5
29.9 – 33.1	24	31.5
33.1 – 36.5	25	34.8
36.5 – 40.4	26	38.4
40.4 – 44.6	27	42.5
44.6 – 49.3	28	46.9
49.3 – 54.5	29	51.9
54.5 – 60.3	30	57.4
60.3 – 66.6	31	63.4
66.6 – 73.5	32	70.1

Fig. 3—Quantization level and quantized voltage vs input voltage.

The maximum sampling rate of a waveform by the quantizer can be obtained by means of (19). The maximum time per quantization, T_q, is

$$T_q = N\Delta T = \frac{\Delta T}{2S} \log R. \tag{21}$$

Then the maximum sampling rate, F, is

$$F = \frac{1}{T_q} = \frac{2S}{\Delta T} \frac{1}{\log R}$$

$$F = 2Sf \frac{1}{\log R} \tag{22}$$

where f = frequency of the pulse generator.

This equation allows for no recovery time of the quantizer between samples. Allowing, conservatively, a recovery time equal to the maximum quantization time gives for the sampling rate, F'

$$F' = Sf \frac{1}{\log R}. \tag{23}$$

For $S=.05$, $f=1\times10^6$, $R=30$

$$F' = \frac{.05 \times 10^6}{\log 30} = 14.7 \times 10^3 \text{ samples/sec.}$$

Proper quantization of an input voltage sample will occur over the voltage range R defined by the lower limit E_0 and the upper limit E_N where $E_N/E_0=R$. Extremely large quantization errors can occur when the voltage samples are outside of this range. The range limitation can be eliminated by the use of voltage attenuators in a system such as shown in Fig. 4. Here the

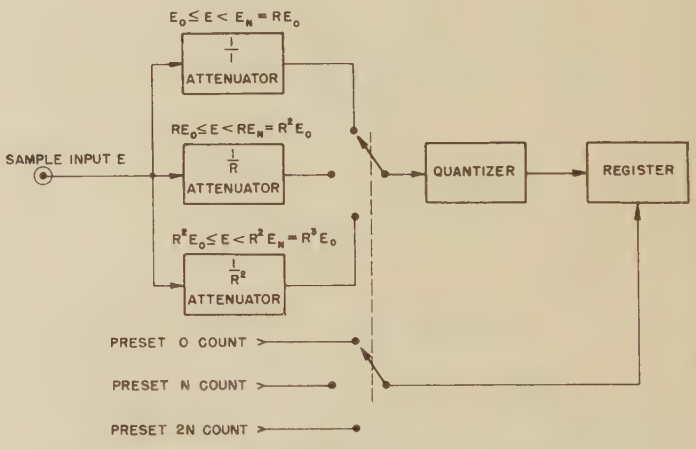

Fig. 4—Logarithmic quantizer with dynamic range of R^3.

voltage range has been increased to R^3. The attenuation ratios are $1/1$, $1/R$, $1/R^2$, $1/R^3$, etc. The range of quantization may be increased as much as is desired by paralleling the suitable range attenuators.

If the voltage sample E is in the R^m range and is such that

$$R^mE_n \leqq E < R^mE_{n+1}$$

where m is an integer, then using (16)

$$r^{mN}r^{n}E_T \leqq E < r^{mN}r^{n+1}E_T$$

$$r^{mN+n}E_T \leqq E < r^{mN+n+1}E_T. \qquad (24)$$

The correct quantized output for E is $nM+n$, the exponent of r in the left hand term of (24). The quantizer by itself will operate correctly only in the range for which $m=0$. Its output will be the number n. When $m\neq 0$, the correct quantized output can be obtained by placing the proper attenuator on the sample input to the quantizer and presetting a count of mN into the quantizer register. This is particularly simple when N is a power of 2. Automatic systems to accomplish the change of range can be readily attained with voltage comparators and selection gates.

Any quantity which can be converted into an analog voltage can be quantized logarithmically. In its present application the quantizer is used to measure with a maximum error of 5 per cent the time between two pulses whose separation may vary from 1 to 14,700 μsec. Three linear sweeps, 1–24.5 μsec, 1–600 μsec, 1–14,700 μsec are started simultaneously when the first pulse occurs. The second pulse terminates the sweeps and starts the quantization. If the second pulse occurs less than 24.5 μsec. after the first pulse, then no count is preset into the register, if the second pulse occurs between 24.5 and 600 μsec after the first, a count of 32 is preset into the register, if the second pulse occurs between 600 and 14,700 μsec after the first, a count of 64 is preset into the register.

Circuit Design

The quantizer is designed to work with voltage samples ranging from 3.0 volts to 73.5 volts and a minimum duration of 0.5 μsec. A block diagram is shown in Fig. 5, the circuit schematic in Fig. 6, and a timing diagram in Fig. 7, on the following page.

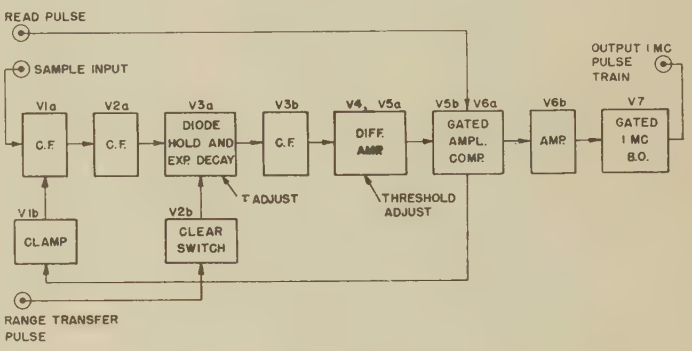

Fig. 5—Block diagram of quantizer.

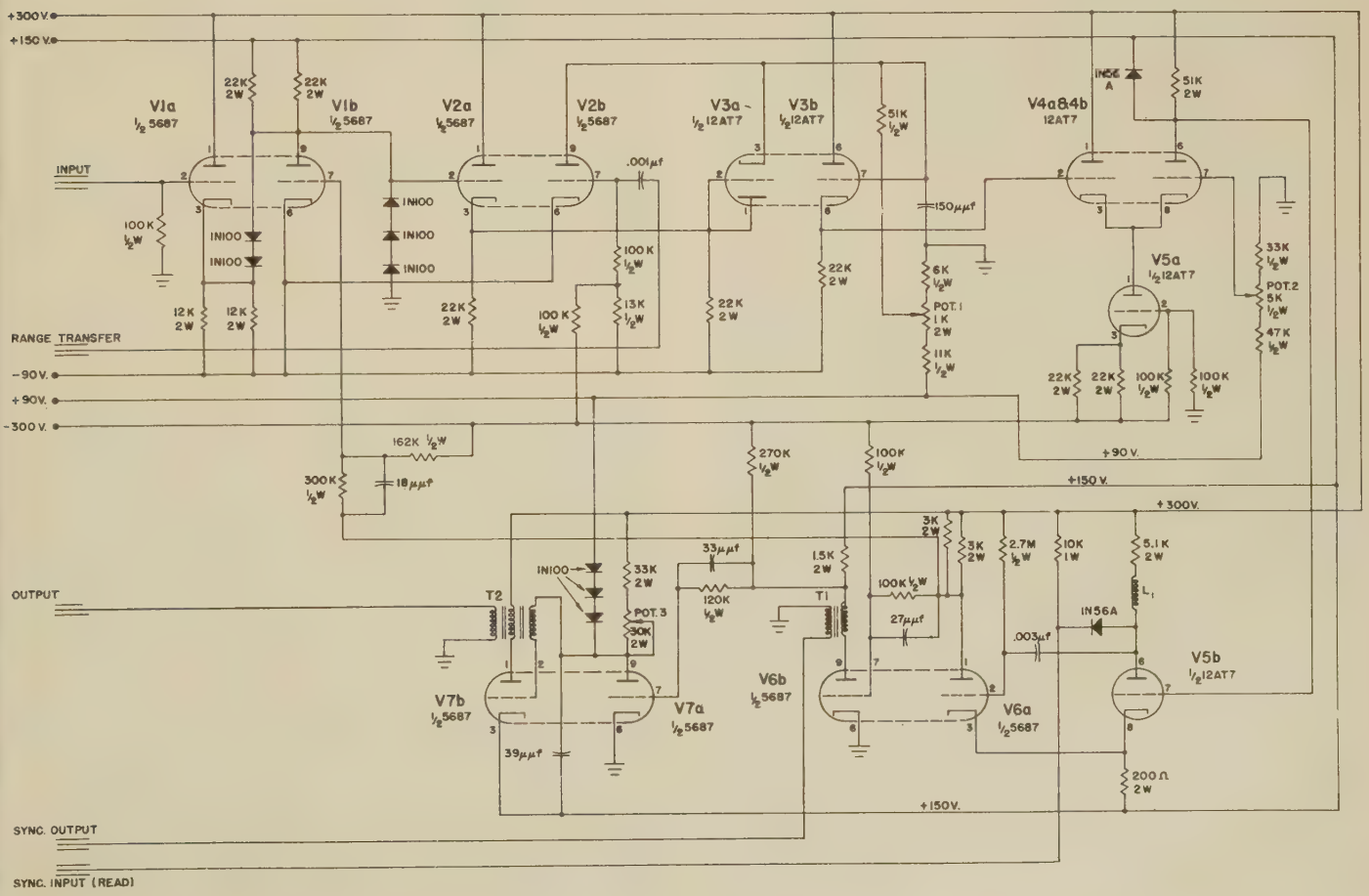

Fig. 6—Log quantizer.

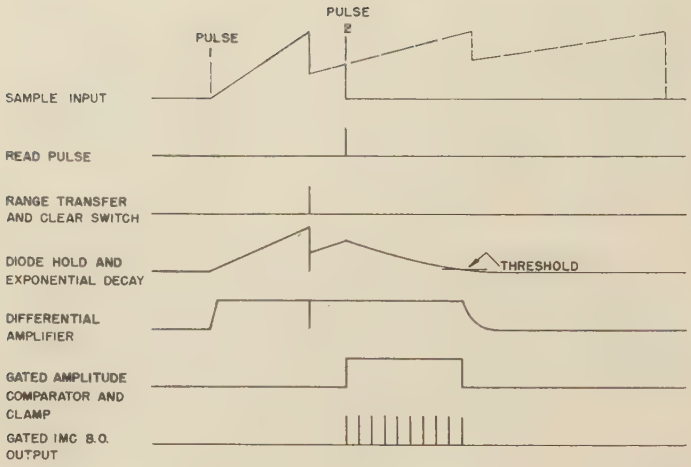

Fig. 7—Timing diagram.

The input cathode follower, *V1a*, is designed for fast rise times in order to be able to handle pulses of duration as short as .5 μsec. During the interval of quantization the output of this cathode follower is clamped to ground by $V1_b$ to prevent any charging of the decay circuit.

The second cathode follower, *V2a*, also is designed for fast rise time and provides a low impedance source for charging the exponential decay circuit.

The resistance-capacitance decay network is charged through diode connected *V3a*. A clear switch, *V2b*, provides for fast discharge of this circuit when the sweep input transfers from one range to the next.

The exponential decay waveform is amplified in the differential amplifier, *V4*, and *V5a*, after a stage of buffering the cathode follower *V3b*. Threshold adjustment for in following amplitude comparator is provided for in this amplifier by means of an output voltage level control.

The amplitude comparator, *V5b* and *V6a*, is a gated ac coupled comparator. The gating or read pulse is of .1 μsec duration and is derived from the second pulse of the pulse pair whose separation is being measured. If the voltage at the grid of the comparator exceeds the threshold level, the comparator will be turned on when the read pulse occurs and will be turned off when the voltage at the grid falls below the threshold level.

The output of the amplitude comparator is amplified in *V6b* and fed to a gated 1 mc blocking oscillator, *V7*. The output of this blocking oscillator is the chain of pulses whose number is proportional to the logarithm of the input voltage sample.

In all pulse circuits timing will be affected by unavoidable delays in pulse transmission. In the quantizer there is a delay between the start of the exponential decay and the "on" triggering of the blocking oscillator. There is also a delay between the time the exponential decay falls through the threshold level and the "off" triggering of the blocking oscillator. These delays are constant regardless of the magnitude of the voltage sample. Because of the nature of the exponential decay, the delays are equivalent only to a change in the threshold level. Their effect can be completely eliminated by a simple adjustment of the threshold level. Delay lines are not necessary.

TRANSITION VOLTAGE	NUMBER OF PULSES 5 % QUANT.
3.00	0
3.32	1
3.66	2
4.05	3
4.48	4
4.95	5
5.47	6
6.04	7
6.68	8
7.38	9
8.15	10
9.01	11
9.96	12
11.0	13
12.2	14
13.4	15
14.9	16
16.4	17
18.2	18
20.1	19
22.2	20
24.5	21
27.1	22
29.9	23
33.1	24
36.5	25
40.4	26
44.6	27
49.3	28
54.5	29
60.3	30
66.6	31
73.5	32

Fig. 8—Number of pulses vs transition voltage.

Experimental Results

The quantizer was calibrated under dc conditions by varying the input voltage level. Adjustments are made in two steps. First, the input pulse is set at 3.32 volts amplitude and *P2* is adjusted until one pulse is observed at the output. The input pulse is then set at 73.5 volts, and *P1* is adjusted until 32 output pulses are observed.

The voltage increment corresponding to each quantization interval is determined by measuring the input voltage at which the number of output pulses changes by one. Fig. 8 shows the theoretical transition voltages for 5 per cent quantization. Results of a typical run at 5 per cent quantization settings are shown in Fig. 9. The straight line passes through the theoretical quantization voltages. The departure of the experimental points from the theoretical line is caused primarily by nonlinearities in the cathode followers. The decay waveform may also differ slightly from the pure exponential. By proper adjustment of the threshold voltage, the errors

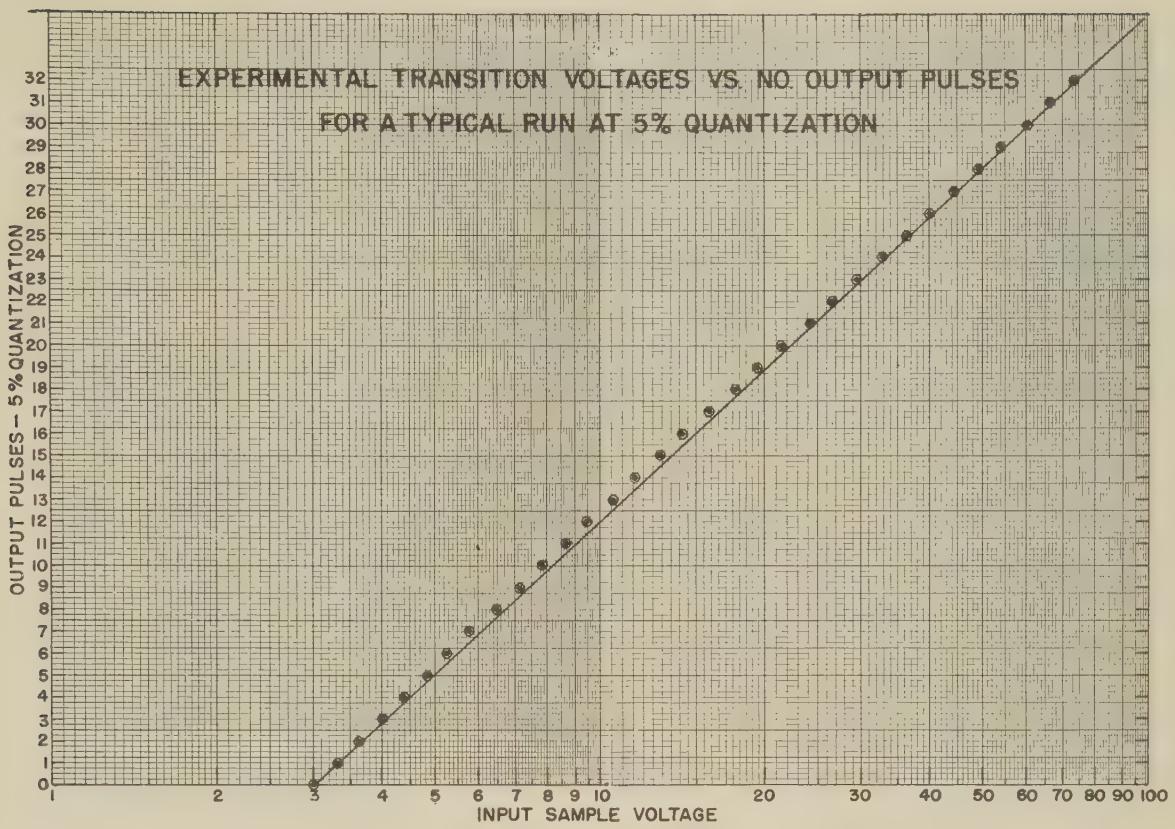

Fig. 9—Experimental transition voltages vs no. output pulses for a typical run at 5 per cent quantization.

in these transition voltages can be kept to less than 2 per cent. Long term variations in plate and filament voltages produce variation in the threshold voltage, E_T. By the use of 1 per cent regulated filament supplies and conventional regulated plate power supplies the long term drift in the threshold voltage is held within 1 per cent. This per cent error in E_T produces the same error in the transition voltages. The over-all error in the quantization at present, therefore, is somewhat less than 8 per cent for nominal 5 per cent quantization.

Other Applications

Multiplication of any two quantities expressible as analog voltages is performed by logarithmic quantization of the inputs and their addition in a counter. The sum is the logarithm of the product of the two quantities. Division is performed by subtraction of the logarithms. In this connection it should be noted that the quantizer takes the logarithm of the ratio E/E_T. Therefore, in multiplication of E_a and E_b

$$\log \frac{E_a}{E_T} + \log \frac{E_b}{E_T} = \log \frac{E_a E_b}{E_T^2} \tag{25}$$

and in division

$$\log \frac{E_a}{E_T} - \log \frac{E_b}{E_T} = \log \frac{E_a}{E_b} \cdot \tag{26}$$

If E_T is made equal to ϵ in the design of the quantizer, multiplication of E_a and E_b yields

$$\log \frac{E_a}{\epsilon} + \log \frac{E_b}{\epsilon} = \log E_a E_b - 2. \tag{27}$$

If E_T is made 1,

$$\log \frac{E_a}{1} + \log \frac{E_b}{1} = \log E_a E_b \tag{28}$$

The quantizer can be used to sample and code a complex wave. Sampling is performed by synchronizing the quantizer at evenly spaced intervals equal to one over twice the signal bandwidth. The quantization accuracy range, and timing interval determine the upper limit on the bandwidth of the signal which the quantizer can handle, as shown in (23) where F' is twice the bandwidth of the sampled signal.

The quantizer will permit measurement of amplitudes of pulses whose durations are as short as one-half μsec. Repetitive pulse trains are not necessary since only a single pulse is sued for the measurement.

Acknowledgment

The authors wish to express their appreciation to W. S. O'Hare for his helpful suggestions in the development of this equipment and to H. Snyder for his careful work in its construction and calibration.

High Density Williams Storage*

S. Y. WONG†

Summary—In this study, an investigation was made to discover methods of storing more bits on a Williams tube than can be stored by conventional methods. Read-around was ignored because the object was to explore the Williams tube as a secondary memory for non-random access operations. Proceeding on this basis, it was found that a four-fold increase in packing is possible with established techniques, and an even greater increase with other methods described in this paper. Such a memory is more versatile than a magnetic drum, as shown by the example of machine organization presented in this paper.

Introduction

ONE GREAT DRAWBACK of the Williams storage system [1] is the read-around, or redistribution, trouble when used as a random access memory. It is well known that read-around can be improved by increasing the spacing between bits. In view of this fact, it can also be aruged that if read-around can be restricted by using special modes of operation, packing can be increased. The investigation was divided into the following general phases:

1) Most operating Williams storage systems assign two neighboring locations to store one bit of information [2]. Each of these locations occupies an area having a diameter approximately equal to that of one spot of the beam. If only one position is bombarded, this position will contain a positive charge because the number of secondary electrons released exceeds the number of primary electrons arriving. If the two positions are bombarded in succession, the first position will be negatively charged because of the deposition of secondary electrons when the second position is bombarded. Thus two kinds of signals can be stored in the first position. The second position really does not store any information. If this second position can be shared between two neighboring bits, some improvement in packing should result.
2) The read-around and packing density trade was investigated by using the techniques of an operating Williams memory. The packing was increased until the Williams tube failed to store a prescribed sequence of ones and zeros.
3) The geometry of the cathode ray tube was also briefly investigated. For a given size beam spot, it is obvious that the larger the screen size, the greater the number of bits that can be stored on a single Williams tube. Experiments were carried out by using different sizes of cathode ray tubes.

Long term stability was not included in the investigation because this calls for much more elaborate equipment. Most of the experiments described in this paper were done on an exploratory basis, and used relatively simple equipment of conventional design; details of the equipment used, therefore, are omitted.

It was envisioned that with increased packing, and employed in a role similar to that of the magnetic drum, the Williams system should be more flexible, and may even be competitive in cost. The greater flexibility of the Williams system is demonstrated by an example of a hypothetical machine organization.

Experiments and Results

Using the double-dot system, and circuitry similar to that in the Institute for Advanced Study machine [3], it was found possible to store successfully a mixed pattern (a random mixture of ones and zeros) of 64×64 on the 3-inch RCA C73621 cathode ray tube (very similar to the 6571 storage tube). This is done by briefly introducing some noise into the system by mechanically tapping the signal amplifier. Five sample tubes were tested, and each was found capable of storing the mixed pattern, as observed with a long-persistence oscilloscope, with no visible change of the pattern over many regeneration cycles. Furthermore, it was found that the raster could be shrunk from normal size (largest possible for the tube) to approximately $1\frac{1}{2} \times 1\frac{1}{2}$ inches.

Since according to Williams and Kilburn a spot diameter is sufficient to isolate neighboring bits, it was decided that a three-dot system might be a practicable means of increasing the packing. Fig. 1 shows a comparison between the two-dot and the three-dot systems.

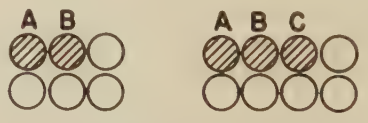

Fig. 1—Relative areas needed by the two-dot system (left) and the three-dot (right).

The shaded areas denote the positions at which the beam is turned on. It can be seen that the three-dot system provides an increase of 50 per cent or more in packing.

In the three-dot system, A and C each contain one bit of information. The positions are inspected by turning the beam on at A and then at C; their contents are recorded in two flip-flops. Fig. 2 shows the amplified

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† Philco Corporation, Philadelphia, Pa.

output signals for the four possible combinations. The contents of A and C are destroyed after application of the inspection pulses. The beam is then turned on at B to make both A and C contain ones. The beam is again turned on at A to produce a zero at A if A originally contained a zero; the same applies to C. A 16×64 raster of this type successfully stores the four combinations of contents of A and C. There is room for two more such rasters on the face of the C73621 cathode ray tube. So it is believed that a 48×64 raster of this type is possible.

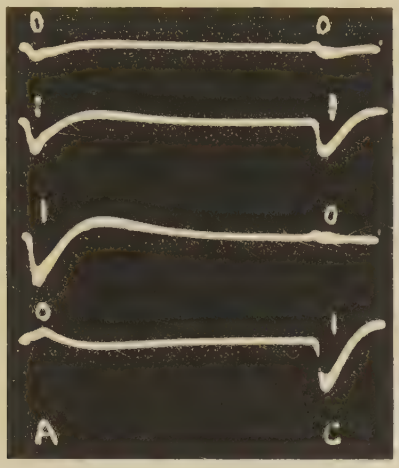

Fig. 2—Output signals with the 3-dot system.

The remaining series of experiments explored the packing density per tube by using various sizes of cathode ray tubes. Using the two-dot system throughout, one each of the 5CP1A, 7VP1, and 17BP4A tubes were tested. Both the 5CP1A and the 7VP1 can barely store the 64×64 raster when the raster is of the maximum permissible size. Since there is no significant advantage in using either of these two types, as far as packing is concerned, they were given no further consideration.

A mixed pattern on a 16×128 raster was stored on a 17BP4A. This raster can be moved to store on different portions of the tube surface. It is necessary to readjust the focus of the tube when such a move is made. By careful manipulation, the raster can be made to occupy a space of only $9/16\times6$ inches if it is placed in the center. The spot diameter of the 17BP4A tube which was tested is approximately 1.7 times that of the C73621 storage tube, while the screen area of the larger tube is several times that of the smaller tube. Therefore, the increase in packing per tube is greater with the 17BP4A or even larger tubes. Deflection defocusing of the larger tubes is quite severe, although methods of correction are straightforward. Without focus correction, an attempt to store a 128×128 raster showed that no one focus adjustment is satisfactory for the entire raster. This point was not pursued further because the focus correction circuit is external to the cathode ray tube, and was not the subject of this investigation.

To demonstrate the usefulness of a non-random access Williams storage system, an example of machine organization, shown in Fig. 3, is offered.

It is necessary, of course, to have a random access memory for any serious computation. The organization diagram indicates that the non-random access Williams memory communicates with three different units. Basically, the Williams memory regenerates its contents in a sequential manner. It is intended that the information exchange between the Williams memory and the other three units be limited to relatively long sequences. The higher the rate of occurrence, the longer the sequences should be, in order to insure regeneration. Input-output devices such as punched cards or tape have relatively low rates. In these cases, it is only necessary to interrupt the regeneration routine whenever a word is to be communicated between the Williams memory and the input-output devices. Most input-output routines consult the addresses of the Williams memory in sequence at a low rate; it is therefore possible to interlace the input-output routine with other routines imposed on the Williams memory without interference with each other.

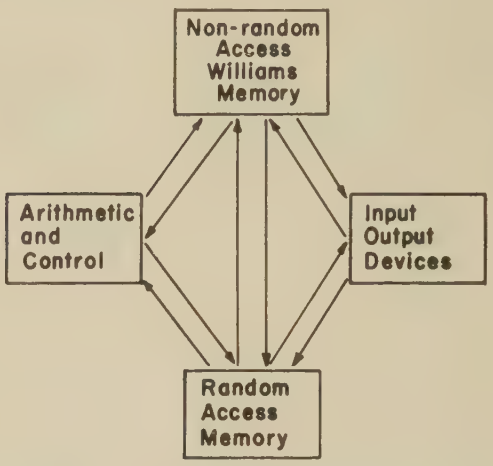

Fig. 3—An example of machine organization using a non-random access Williams memory system.

If the communication between the Williams memory and the random-access memory is limited to blocks of information, it is practicable to allow a jump in the regeneration routine to the starting address of the block. This, then, also becomes the new regeneration routine. A time delay equal to the time required for one regeneration cycle of the entire memory is set in motion in such a manner that this time delay must expire before any further jump can be made, thus insuring a low read-around. This limitation actually is not too important, considering the fact that usually, after such a transfer, some time is devoted to arithmetic operations on the transferred words. Orders or data are quite often referred to in a sequential manner. These references, however, usually occur at a much higher rate and may equal or even exceed the speed of the Williams memory. In this case it is permissible to interrupt the regeneration routine, but not to alter it. However, a counter is needed to keep track of the work sequences, and a time delay similar to that mentioned above is set in motion so as to insure low read-around.

The foregoing example shows that the Williams memory, when operated in the manner described, is more flexible than a magnetic drum. It is also possible to eliminate some of the access time normally unavoidable on the drum, unless serious coding requirements are imposed.

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[3] Goldstine, H. H., Pomerene, J. H., and Smith, C. V. L., Progress Report, Electronic Computer Project.

Correspondence

This section is devoted to brief reports on new ideas in the computer field, comments of timely interest to PGEC members, or comments on recent papers in the TRANSACTIONS ON ELECTRONIC COMPUTERS. Communications should ordinarily be limited to 1,000 words in length. The delay between submission of the communication and its publication will be held to a minimum. Authors are invited to send two copies of appropriate material to the Editor.

A Decimal Code for Analog-to-Digital Conversion

Consider the following binary-coded representations for the ten decimal digits:

P	A	B	C	D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	1	0
5	1	1	1	1
6	1	1	1	0
7	1	1	0	1
8	1	1	0	0
9	1	0	0	1

P'	A	B'	C'	D'
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	1	0
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	1	0

P''	A	$\overline{B}$	$\overline{C}$	D
0	0	1	1	0
1	0	1	1	1
2	0	1	0	0
3	0	1	0	1
4	0	0	0	0
5	1	0	0	1
6	1	0	0	0
7	1	0	1	1
8	1	0	1	0
9	1	1	1	1

The representation scheme $P'=AB'C'D'$ (shown in the center above) is a constant weight type of binary-coded decimal numbering system[1] wherein P' can be evaluated by means of the formula

$$P' = 5A + 2B' + 2C' + D'$$

when 0's and 1's are substituted for the letter symbols.

The left-hand code, $P=ABCD$, is identical with P' in the A digit. For the remaining binary digits, however, $B'=B$, $C'=C$, and $D'=D$ when $A=0$, but $B'=\overline{B}$, $C'=\overline{C}$, and $D'=\overline{D}$ when $A=1$. ($X'=\overline{X}$ means that when X is 0, X' is 1, and when X is 1, X' is 0.)

The latter code is of special interest because the A, B, and C columns each contain five 1's in sequence. It is easily seen that, in a digitizer of the reading type (which encodes an "analog" quantity by means of commutator segments and brushes or the functional equivalents), this 4-bit code can be generated with only two rows or zones of commutator segments per decimal digit, relying on three different suitably displaced brushes to generate A, B, and C.

Variants of the code P (for example, the right-hand code P'') which are derived by interchanging the vertical columns, and/or interchanging 0's and 1's in one or more columns, and/or by cyclic reassignment of the Arabic numerals corresponding to code combinations without changing their relative sequences, can likewise be generated with only two rows of commutator segments. Variants which omit the 0000 and 1111 combinations are sometimes desirable.

A problem which always crops up in the design of reading-type coders is that of possible transition errors at values of the analog for which changes occur in the numerical representation (i.e., at quantum boundaries).[2,3] Some transition errors with the codes of the type P are smaller than with many other codes because the maximum number of bit changes which occur when decimal digit changes is two; on the other hand, the necessity for the A, B, and C brushes to be positioned accurately, and in a special manner, introduces a possibility of a new type of transition error, especially hard to control in the case of the "fine" digits of a many-place number. Fortunately, boundary effects, as well as the effects of inexact machining of commutators and brushes, can be minimized with a logical detenting scheme which enables the D brush alone to decide between uncertain readings in the vicinity of quantum boundaries.

Logical detenting for the described binary-decimal codes can be accomplished by making the conductive segment provided to generate A, B, and C somewhat smaller than five times the size of the associated D segments as shown in Fig. 1. Two brushes are

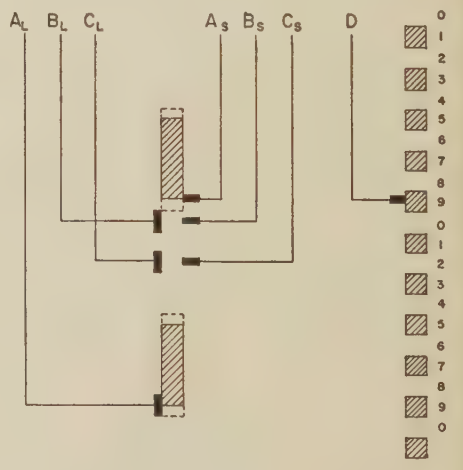

Fig. 1.—Brush and commutator arrangement.

then provided for each of the digits A, B, and C. One set of brushes, A_S etc., is too small in size to compensate for the fact that the cooperating commutator segment is undersized. A_L, B_L, and C_L, however, are large enough to over-compensate for this reduction. Note now, that, as we scan the sequence of combinations in code P, changes in A are always accompanied by *like* changes in D, but changes in B and C are always accompanied by *converse* changes in D. We therefore combine the seven electrical outputs

[1] G. S. White, "Coded decimal numbering systems for digital computers," PROC. IRE, vol. 41, pp. 1450–1452; October, 1953.

[2] R. W. Sears, "Electron beam deflection tube for pulse code modulation," *Bell Sys. Tech. Jour.*, vol. 27, pp. 49–57; January, 1948.

[3] B. Lippel, "A high-precision analog-to-digital converter," *Proc. N.E.C.*, vol. 7, pp. 207–215; February, 1952.

shown in Fig. 1 in circuits which perform the following logical operations to get unambiguous 4-bit representations of the decimal digits:

$A = A_s + A_L D$; *i.e.*, "A is the logical combination of A_s or (A_L and D)"

$B = B_s + B_L \overline{D}$

$C = C_s + C_L \overline{D}$

$D = D$

If we use the code variant P'' (obtained from P by interchanging 0's and 1's in both B and C columns), the logic required for detenting is even simpler, *viz:*

$$A = A_s + A_L D$$
$$B = B_s + B_L D$$
$$C = C_s + C_L D$$
$$D = D$$

Code P'' also has some advantage in more uniform spacing of A, B, and C brushes. In a coder which uses true contact switching, some of the logic can be performed by means of duplicate A, B and C commutator segments, serving "large" and "small" brushes individually, and series-connected contacts.

The codes cited are preferred over cyclic code sequences (in which exactly one binary digit changes at each transition) because each group of four binary digits stands for one particular decimal digit in a many-place decimal number, regardless of the digits standing in other decimal places. With these codes, therefore, a simple switching matrix alone can serially translate each binary group into decimal terms, or the binary code groups can operate typewriters directly to print Arabic numerals without the use of a translator. Cyclic codes always require translators operative on all digits collectively.

Referring to code P or code P'' as extended to two or more decades, we note that the relationship between the A digit of one decade to the D digit of the next higher decade is similar to that between successive digits in the natural binary numbering sequence, *viz:* A_1 is alternately 0 and 1 (over 5-quantum intervals), and D_{10} is likewise alternately 0 and 1 (over 10-quantum intervals); whenever A_1 goes from 1 to 0 as the number increases, D_{10} changes simultaneously; when A_1 changes in the reverse direction as the number increases there is never a change in D_{10}. Logical detenting over a number of encoded decimal places is therefore accomplished by combining the above detenting principles with the V-scan technique used for true binary coding.[4]

Two brushes are employed to generate D in the tens place and higher places. One brush is offset in the direction of decreasing numbers and is utilized when the previous decade's A digit is a 1; the other brush is offset equally in the direction of increasing numbers and is brought into play when the previous A is 0.

Logical detenting of bits and decades greatly reduces the amount of accurate workmanship required in reading-type digitizers because only the commutator segments in the units decade must be accurate $\pm 1/2$ quantum. Succeeding decades may be constructed with tolerances proportional to the weighting factors for the generated decimal places.

The above principles can also be put to use for decimal revolutions counters, constructed with identical stages, and geared up with gearing of indifferent accuracy.[5,6] The ease with which the generated codes are converted to constant-weight codes simplifies decoding to realize an analog proportional to the count; this makes the system particularly attractive for self-balancing potentiometers with digital output.

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[4] R. H. Barker, "Measurement of angle using the binary digital scale" (See A. Tustin, "Automatic and Manual Control," Academic Press, Inc., New York, pp. 561–566; 1952.)

[5] A. D. Scarbrough, "An analog-to-digital converter," Trans. IRE, vol. EC-2, pp. 5–7; September, 1953.

[6] W. H. Libaw and L. J. Craig, "A Photoelectric decimal-coded shaft digitizer," Trans. IRE, vol. EC-2, pp. 1–4; September, 1953.

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PGEC News

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Committee Chairmen

The following is an up-to-date list of the Chairmen of various PGEC Standing Committees. It is published here so that members interested in various phases of PGEC activities may contact those listed.

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R. W. Melville, *Chairman*
Stanford Research Institute
Menlo Park, Calif.

Publications

Werner Buchholz, *Chairman*
IBM Engrg. Lab.
P. O. Box 390
Poughkeepsie, N. Y.

Awards

J. P. Eckert, Jr., *Chairman*
Director of Engrg.
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2300 West Allegheny Ave.
Philadelphia 29, Pa.

Student Activities

Harry H. Goode, *Chairman*
Willow Run Res. Ctr.
Willow Run Airport
Ypsilante, Mich.

Meetings

Inactive at present.

Sectional Activities

Stanley B. Disson, *Chairman*
Burroughs Corp.
Research Center
Paoli, Pa.

Constitution and Bylaws

Darrin H. Gridley, *Chairman*
USN Res. Lab.
Radio Div. III
Washington 25, D. C.

Ad Hoc Committee

Membership Survey[1]

William L. Martin, *Chairman*
Marchant Calculators, Inc.
Oakland 8, Calif.

[1] This committee is engaged in preparing a questionnaire to circulate among the membership in order to determine which subjects are of greatest interest to the computer field as a whole.

Albuquerque-Los Alamos

The Albuquerque-Los Alamos section has decided not to hold meetings this year due to the fact that the entire membership is composed of persons who work in the same division at the Sandia Corporation.

PGEC Directory

Copies of a Directory listing the national and chapter officers and committee chairmen of the PGEC are available from the editor of this column upon request.

Meetings

January (1956)

9–10, *Second National Symposium on Reliability and Quality Control in Electronics*, Hotel Statler, Washington, D. C. For further information—V. Wouk, Beta Electric Corp., 333 East 103rd Street, New York 29, N. Y.

19–21, *National Simulation Conference*, Dallas, Texas. Sponsored by Dallas-Fort Worth Chapter of IRE Professional Group on Electronic Computers.

30, *AIEE Winter General Meeting*. Ends February 3rd. Hotel Statler, New York, N. Y.

February (1956)

8–10, *Western Joint Computer Conference*, San Francisco, Calif. For further information—Byron J. Bennett, Chairman Tech. Program Committee, Stanford Research Institute, Stanford, Calif.

Reviews of Current Literature

It is the intention of this section to review articles that have been published since January 1, 1953, and to publish eventually reviews of all books pertaining to the computer field. Authors can be of considerable assistance in this review process by sending two reprints of their articles to H. D. Huskey, Department of Electrical Engineering, University of California, Berkeley, California. The editors wish to express their gratitude to the reviewers who, through their efforts, make this section possible.

H. D. Huskey, Editor

GENERAL

55-116

The Computer Directory 1955—(*Computers and Automation*, vol. 4, pp. 6–150; June, 1955.) This issue is devoted entirely to the Computer Directory which is divided into three parts: Part 1, "Who's Who in the Computer Field"; Part 2, "Roster of Organizations in the Computer Field"; and Part 3, "The Computer Field: Products and Services for Sale."

Gordon Morrison

55-117

PGEC Student Activities and Education in Computers—H. H. Goode. (TRANS. IRE, vol. EC-4, pp. 49–51; June, 1955.) Results of a survey are tabulated to indicate the electronic computer activities and facilities at 91 universities in the United States and Canada. For each university, the tabulation shows whether or not analog and digital computers are available, with available machines classified as general purpose or special purpose computers. Computer facilities planned, but not in operation, are also indicated. The survey includes the status of courses in orientation, in design, and in operation of electronic computers. The name and title of a faculty member who can supply information about electronic computation at each school are given. The survey also reveals, in the field of electronic computing, whether or not graduate courses are offered, assistantships are available, advanced degrees are granted, and regular seminars held. The survey, which meets the objective of collecting data about specific schools for students interested in computing, is of general interest because it shows the rapid development of computation facilities in universities.

Leslie H. Miller

55-118

Automation—A Survey—R. J. Bibbero. (*Elect. Engrg.*, vol. 74, pp. 775–780; September, 1955.) This article gives a brief history of items which may be considered to be automatic controls, touching on such items as the human body's mechanism for temperature regulation, and including ancient items, starting in the third century B.C. Production line automation and job shop automation are contrasted. Digital control of machine tools is discussed. Recent developments in the automation of assembly of electronic equipment are presented. Process control is reviewed, followed by a brief discussion of the use of digital equipment in the automation of business data processing.

Harry T. Larson

55-119

Mathematics, the Schools and the Oracle—Alston S. Householder. (*Computers and Automation*, vol. 4, pp. 6–9; July, 1955.) Every person active in the computer field finds it necessary from time to time to explain to laymen the continued necessity for mathematicians in the world of "giant brains." Such a discussion invariabiy requires an introduction to the concept of programming and to mathematical analysis. This article, which is a reprint of a talk delivered by the author, provides an excellent presentation of this information.

Gordon Morrison

55-120

Some Applications of Symbolic Logic—James C. Hetrick. (*Ind. Math.*, vol. 5, pp. 117–130; 1954.) This is essentially an expository paper in which the author points out how the advent of large scale computers has influenced the applications of symbolic logic. Some interesting illustrative problems in class algebra are given and some truth tables are constructed. The author introduces a modified notation to simplify the mechanics of handling these syllogisms. Among the machines which have been used to construct truth tables are the Kalin-Burkhart Logical Truth Calculator, the Burroughs Truth-Function Evaluator, the California Digital Computer and the Electro Data Computer.

Samuel D. Conte

55-121

A Symbolic Method for Synthesis of Two-Terminal Switching Circuits—D. Zeheb and W. P. Caywood. (*Comm. and Elect.*, No. 16, pp. 690–693; January, 1955.) A system for designing two-terminal relay switching networks is described. Although Boolean algebra notation is used to specify the switching functions, the design method is largely schematic. Relay transfer points are included as an integral part of the system. The design procedure is extended to make use of "don't care" terms in order to achieve the minimum number of components. Three examples are worked out in detail.

R. K. Richards

55-122

A Rectifier Algebra—D. H. Schaefer. (*Comm. and Elect.*, No. 16, pp. 679–682; January, 1955.) An algebra is described which is claimed to be of assistance in the design of circuits containing rectifiers. The algebra is based on two functions of a and b, where one function is equal to the more positive of a and b and the other function is equal to the more negative of a and b. Several circuits containing diodes are presented to illustrate the relationship between circuits and the notation. One example is given to show application of the algebra in circuit analysis. Unfortunately, example is so simple and easily solved by ordinary methods that usefulness of the algebra is not clear.

R. K. Richards

55-123

A Logarithmic Voltage Quantizer—E. M. Glaser and H. Blasbalg. (*Proc. WESCON Computer Sessions*, August 15–27, 1954, Los Angeles, Calif., pp. 19–28; 1955.) The time required for the output of an RC network to decay exponentially to a reference value is related linearly to the logarithm of the initial voltage. This initial value is established by a voltage sample the occurrence of which triggers both a pulse and a one-megacycle fixed-frequency oscillator. The pulse is cut off when the reference value is reached, resulting in a pulse-duration representation of the logarithm of the original voltage sample. Counting the number of oscillator cycles occurring while the pulse endures then affords a quantized measure of this logarithm. Detailed circuit diagrams are included and applications are mentioned. Voltage samples must be between 3.3 and 100 volts. Samples may be converted at a rate up to 29,400 per second at 10 per cent resolution; lower rates permit finer resolution. Amplitudes of inputs of duration as short as one-half microsecond may be measured.

Louis B. Wadel

55-124

Networks for Digital-to-Analogue Shaft-Position Transducers—S. J. O'Neil. (*Comm. and Elect.*, No. 15, pp. 456–466; November, 1954.) Several networks are described for translating a set of digital signals to approximations of sine functions to be applied to the stator windings of two-phase or three-phase resolvers or synchos. The object is to convert a relay contact digital representation of a quantity to a shaft-position analog representation. An analysis is made of the errors involved. Extensions of the concepts, together with theoretical accuracies achievable, are also presented.

R. K. Richards

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—*The Editor*

ANALOG COMPONENT RESEARCH

55-125

An Analog Multiplier Using Thyrite—L. D. Kovach and W. Comley. (TRANS. IRE vol. EC-3, pp. 42–45; June, 1954.) A commercially available nonlinear resistance element Thyrite (General Electric Cat. No. 839689G1) is used in combination with a linear resistor to provide a circuit element which has a square function characteristic accurate to approximately 1.5 per cent. Because Thyrite is anti-symmetrical, diodes are utilized to obtain an output polarity which is the same for either sign of input. However, for some applications such as simulating a square-law damper, the anti-symmetrical characteristic is applicable and the diodes can be omitted. For convenience, all of the components that comprise a squaring circuit element are mounted on a plug-in unit. These units can be inserted in a computer patchboard in such a manner that a quarter-square type multiplier can be connected which will have low drift, a frequency response in excess of 1,000 cps and an accuracy which approaches 1.25 per cent.

Charles M. Edwards

55-126

Time-Delay Networks for an Analog Computer—W. J. Cunningham. (TRANS. IRE, vol. EC-3, pp. 16–18; December, 1954.) Transfer function of time delay exp $(-sT)$ is approximated by fractions of the form

$$\frac{(s - Z_1)(s - Z_2) \cdots}{(s - P_1)(s - P_2) \cdots}.$$

The symmetry restrictions on pole and zero locations in the s plane are indicated. The corresponding restrictions on phase and attenuation as functions of frequency are then utilized to calculate the location of zeros and poles directly. These locations are then simply related to coefficient settings in the analog computer set-up. The subject matter of this paper is propitious (a necessary substitute for the adjective "timely"). The need for time-delay functions in analog computing is becoming widespread. The author's development is systematic and explicit. His suggestion of cascading simple networks to synthesize more elaborate configurations is useful. Questions which the analog computer man might ask are: 1) Of the various approximation techniques available, does this one provide more rapid identification of the required computer configurations and numerical coefficients? 2) What can be said with respect to stability, noise, and minimization of numbers of components? (The paper proposes an 8-amplifier configuration for a characteristic which could be realized with 3, a fact which adds a lavish air to the method described.) Further discussion of this paper appears in TRANS. IRE, vol. EC-4, p. 74; June, 1955.

Don Lebel

ANALOG EQUIPMENT

55-127

A Survey of Electronic Analog Computer Installations—L. B. Wadel and A. W. Wortham. (TRANS. IRE, vol. EC-4, pp. 52–55; June, 1955.) This article presents the results of a survey of the electronic analog computer installations in the United States and Canada. The purpose of the survey was to determine the size of each installation, the number of its personnel, availability of computer facilities to outside organizations, etc. The results are tabulated as to geographic distribution of installations, number of amplifiers in an installation, and the availability classification. Figures present growth information of these computer installations since 1946 when the first one was established. An appendix to the article is a directory of 98 electronic analog computer installations in the United States and Canada.

Cyril P. Atkinson

681.142:621.37:535.32 55-128

Analogue Machine for Calculation of the Complex (refractive) Index of a Body from its Reflection Coefficient—M. Hénon. (*Compt. Rend. Acad. Sci. (Paris)*, vol. 240, pp. 1305–1306; March 21, 1955.) A resistance network is discussed by means of which the phase shift of light reflected by a body can be calculated if the reflection coefficient is known for all wavelengths; the refractive index can hence be determined.

Courtesy of PROC. IRE and *Wireless Engineer*

UTILIZATION OF ANALOG EQUIPMENT

55-129

Accuracy of an Analog Computer—Lee Cahn. (TRANS. IRE, vol. EC-2, pp. 12–18; December, 1953.) This paper presents practical methods of determining accuracy requirements and making comparisons of amplifier and integrator units of general purpose electronic analog computers. The methods given will be useful to people concerned with the problems of determining accuracies and making decisions as to the best method of obtaining a given accuracy with an electronic analog computer. The paper is evidently written with authority obtained from experience. However, in some cases, the author's familiarity with the problem has led him to presume a similar reader experience, with the result that some terms and symbols are poorly defined, and some explanations sketchily presented. The proof in the Appendix puzzled the reviewer. It seemed to depend on the unjustified assumption that a third-order system transfer function was reduced to a second-order transfer function by the gain adjustment that brought the system into stable oscillation. However, the reviewer agreed with the author's conclusion, since application of the stability boundary condition of Nyquist's criterion to the original third-order transfer function will give the author's final expression

$$T = \frac{A}{\omega_n^2 R_1 C_1}.$$

The author dismisses other elements, such as multipliers and function generators, with the statement that they can be handled by obvious extensions of the methods given. The reviewer would like to have seen a discussion of errors in multipliers, where the problem is complicated by the fact that the error is a function of two variables.

A. M. Hopkin

55-130

Automatic Iteration on an Electronic Analog Computer—Louis B. Wadel. (*Proc. WESCON Computer Sessions*, August 25–27, 1954, Los Angeles, Calif., pp. 13–18; 1955.) A method is described whereby an electronic analog computer may be used to obtain automatic solutions of ordinary differential equations requiring a trial-and-error "starting value" of some unknown parameter or initial condition in order to obtain a pre-specified result. The iteration procedure is effected by means of a multi-pole stepping relay which 1) makes a trial solution of the equation, 2) observes the difference between the result obtained and the result desired, 3) applies a correction to the "starting value," and 4) repeats the process until the desired result is obtained. "However, care must be taken to choose a valid and efficient iteration routine for each problem type." The author shows that in some cases, with an improper setup of the correction method, the iteration process may lead to divergence from the true solution. This method may be extremely valuable for obtaining the solutions to certain problems, particularly when a large number of solutions of the same type of equation are required. In many cases a skilled operator could obtain the desired solutions in less time using conventional methods. Many computers would require modifications to obtain the separate HOLD and OPERATE controls required for at least one integrator.

Carl E. Howe

681.142 55-131

A Statistical Method for Solution of the Laplace Differential Equation using Electronic Computers—H. Harmuth. (*Acta Phys. Austriaca*, vol. 9, pp. 27–32; December, 1954.) An electrical analog of the Galton board is used in which the rolling balls are replaced by pulses and the pins by pulse-storage units.

Courtesy of PROC. IRE and *Wireless Engineer*

DIGITAL COMPONENT RESEARCH

55-132

Pulse-Switching Circuits using Magnetic Cores—M. Karnaugh. (PROC. IRE, vol. 43, pp. 570–584; May, 1955.) Design theory is presented for nonstorage loops in digital computers. To facilitate determination of the sense of the em processes a method of representation due to Mayer is used in which the magnetic-circuit elements are replaced by elements of a mirror system. Devices for eliminating output voltage on "shuttling" the core are discussed. Operating frequencies greater than 100 kc are attainable. 31 references.

Courtesy of PROC. IRE and *Wireless Engineer*

681.142:538.221 55-133

A Radio-Frequency Nondestructive Readout for Magnetic-Core Memories—Bernard Widrow. (TRANS. IRE, vol. EC-3, pp. 12–15; December, 1954.) A method is described for detecting the state of the flux in a ferrite core without altering the state of the core. A method of selecting and sensing one

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—*The Editor*

core in a plane of many is also demonstrated. Radio-frequency signals are used to disturb the cores. A frequency of w_1 is applied on a selected X line and a frequency of w_2 is applied on a selected Y line. On a third read winding a difference frequency—among others—appears. The phase of the difference frequency signal varies 180 degrees depending on the direction of the flux in the core. This phenomena is used to identify the state of flux in the core. Experimental results are reported of a constructed single memory plane. The read cycle time was approximately 15 microseconds. The author points out that this may be shortened by using different drive frequencies and by broadening the response of the playback amplifiers. The method described eliminates the noise due to half disturbed currents, as do other nondestructive methods known to the reviewer, and should be applicable to large core planes. The use of rf, however, particularly on core memory arrays, can safely be classed as a disadvantage.

William R. Arsenault

55-134

The Transfluxer—A Magnetic Gate with Stored Variable Setting—Jan. A. Rajchman and Arthur W. Lo. (*RCA Rev.*, vol. 16, No. 2, pp. 303–311; June, 1955.) A description of a device utilizing a magnetic core made of material with a nearly rectangular hysteresis loop and having two or more apertures is given. The device named "Transfluxor" is capable of storing and gating of electrical signals. The output signal can be controlled according to a stored level of magnetization established by a single setting pulse. As a memory device the readout is nondestructive.

T. C. Chen

55-135

Magnetic Elements in Arithmetic and Control Circuits—I. L. Auerbach and S. B. Disson. (*Elect. Engrg.*, vol. 74, pp. 766–770; September, 1955.) Physical and electrical characteristics of square-loop ferromagnetic cores are described here, followed by a description of some basic circuits suitable for use in digital computers. A single-diode unconditional transfer loop is described, and a conditional transfer circuit is presented. With these basic circuits, circuits for the following logical operations are developed: exclusive OR, inclusive OR, and AND. The application of these basic circuits and logical building blocks is demonstrated by descriptions of various types of registers, a "cycle distributor," and a half adder. The use of such devices in digital equipment is discussed, describing reduction in size, weight, and power and increased reliability to be realized from the use of such magnetic elements. The circuitry described here has been operated at 150 kcps. Advantages and disadvantages of this circuitry are discussed briefly, and the future developments in this type of circuitry are briefly considered.

Harry T. Larson

55-136

A Comparison of Metals and Ferrites for High-Speed Pulse Operation—D. R. Brown, D. A. Buck, and N. Menyuk. (*Comm. and Elect.*, No. 16, pp. 631–635; January, 1955.) Various theoretical and practical factors affecting the choice of magnetic material for applications requiring a square hysteresis loop are considered. The conclusion is reached that ultrathin metal-ribbon cores are better for stepping registers and switching circuits, while ferrite cores are better for use in coincident-current memories. A discussion by H. Ekstein, T. L. Gilbert, and the authors is appended. This discussion seems to indicate that a precise theory of the reaction of square-loop materials is not at hand, but that experimental data is in at least approximate correlation with certain theoretical models.

R. K. Richards

621.383.4/.5:546.289 55-137

Germanium Junction Photodiodes—Zh. I. Alferov, B. M. Konovalenko, S. M. Ryvkin, V. M. Tuchkevich and A. I. Uvarov. (*Zh. Tekh. Fiz.*, vol. 25, pp. 11–17; January, 1955.) In the photocell proposed by Shive the direction of the beam of light is parallel to the plane of the n-p junction. In the cell used in the present investigation the light beam is perpendicular to the plane of the junction and passes through a thin layer of n- or p-type Ge. Experiments were carried out to determine the voltage/current characteristics, dependence of current on intensity of illumination, distribution of sensitivity over the surface, spectral distribution of sensitivity, inertia and temperature effect.

Courtesy of Proc. IRE and *Wireless Engineer*

621.383.4/.5:546.289 55-138

Mechanism of Operation of Germanium Photodiodes—S. M. Ryvkin (*Zh. Tekh. Fiz.*, vol. 25, pp. 21–28; January, 1955.) Theory of the operation of an n-p Ge diode as a photocell is given; the fundamental relations are established between the photo-emf, short-circuit photocurrent, and saturation current for the case of operation as a barrier-layer photocell. A general equation suitable for any operating conditions is also derived. Results are given of experiments made to verify the relations obtained, and the efficiency of the diodes used as barrier-layer photocells is discussed.

Courtesy of Proc. IRE and *Wireless Engineer*

537.311.33+621.314.7 55-139

Semiconductors and the Transistor—E. W. Herold. (*Jour. Franklin Inst.*, vol. 259, pp. 87–106; February, 1955.) A general survey with 33 references.

Courtesy of Proc. IRE and *Wireless Engineer*

55-140

A Multistable Transistor Circuit—R. A. Henle. (*Elec. Engrg.*, vol. 74, pp. 570–572; July, 1955.) This article describes a circuit which has multiple statically stable states (theoretically, any number) and uses only two transistors. The basic circuit uses a grounded-base stage whose output feeds an emitter-follower stage, the output of which is fed back to the input of the grounded-base stage. The feedback is positive, and the circuit can be made stable or unstable by making one load resistor larger or smaller than a fixed resistor in the circuit. Circuits using diodes are described for attaining a load line having alternate low resistance and high resistance values. This makes it possible to trigger the circuit from one stable state to the next. Triggering requirements peculiar to this circuit are given, and two suitable triggering schemes are described. It is suggested that the triggering speed can be as fast or faster than conventional circuits using similar transistors. The circuit is not particularly dependent on the characteristics of the transistor used.

Harry T. Larson

55-141

A High-Accuracy Static Time Delay Device Utilizing Transistors—G. F. Pittman, Jr. (*Comm. and Elect.*, No. 17, pp. 54–58; March, 1955.) The term "time delay" in the title and body of this paper does not seem to have the usual meaning and therefore may be misleading. Actually the paper describes a circuit employing square-loop magnetic cores driven by transistors, and a counting action is achieved. The storage core is switched by a succession of very short pulses instead of one heavy pulse of current with the result that a single core together with its pulse-shaping and resetting equipment can be used as a decimal counter. Experimental results are reported wihch describe data obtained from two such counters connected in cascade. (See **55-142**, this issue.)

R. K. Richards

55-142

A Time-Delay Device Using Transistors—G. F. Pittman, Jr. (*Elect. Engrg.*, vol. 74, pp. 498–501; June, 1955.) This article describes circuitry capable of performing counting operations, making use of the voltage-integrating capabilities of cores with rectangular hysteresis loops, and making use of the transistor's negligible voltage drop when conducting and very small leakage currents when blocking. The circuitry described here calls for input pulses of constant volt-time integral. These are applied to a core, which retains the flux level determined by one pulse, adds the next pulse, etc., integrating the input pulses until a definite value of the volt-time integral is attained. At this point the core saturates sharply, and the circuitry notes this, the core is automatically reset, and the resetting operation produces a pulse which may be used to drive a succeeding core. The principles of operation are described, the basic circuitry is given (including a simple pulse-shaping circuit for generating a unidirectional rectangular pulse of fixed volt-time area), and experimental results are described. Consistent operation is obtained over a temperature range of −65 to +70°C. The experiments described appear to have been conducted at 60 cps. (See **55-141**, this issue.)

Harry T. Larson

681.142 55-143

The Logical Principles of a New Kind of Binary Counter—Willis H. Ware. (Proc. IRE, vol. 41, pp. 1429–1437; October, 1953.) This article describes in detail the logical development of a direct-coupled binary counter. The counter uses two flip-flops per stage. One flip-flop is used in the normal manner as

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a storage element of indefinite period. The second has the same properties as the first but is used as storage during the transient count time. The advantage of the design philosophy is that it does not rely upon time-limited storage (such as that produced by configurations of resistance, capacitance and inductance), and thus is insensitive to pulse shapes. As pointed out by the author, these two properties are even more important in the design of asynchronous machines. The chief disadvantage of the method is that it uses more equipment—more vacuum tubes in particular—than the conventional Eccles-Jordan circuitry.

William R. Arsenault

55-144

Some Notes on Logical Binary Counters—R. M. Brown. (TRANS. IRE, vol. EC-4, pp. 67–69; June, 1955.) The author describes a method of logical counting in which each stage of the counter consists of two flip-flops (True and False toggles respectively). Both polarities of the True toggle of a particular stage are used to drive the next higher stage. A survey of the possible connections between True and False toggles of the same stage is given and it is shown that the True toggles' counting is ordinary binary, whereas the False toggles count is some variety of the well-known Gray-code. The counting of the True toggles can be made additive or subtractive by interchanging their outputs, as far as the driving of the next higher stage is concerned.

This scheme requires one double-sided input for its activation. A more elaborate scheme for counting is given at the end of the article in which two double-sided inputs are needed, 90° apart in phase. Stepping up the counter by one requires a complete cycle of the input variables; *i.e.*, four elementary time intervals. An outstanding feature of this scheme, however, is that additive or subtractive counting depends no longer on interchanging outputs, but on the order of the input signals. The author suggests the use for determining the position of a shaft whose direction of motion may be reversed.

C. S. Scholten

55-145

A Variable Binary Scaler—D. B. Murray. (TRANS. IRE, vol. EC-4, pp. 70–74; June, 1955.) Flip-flop binary counters can be constructed both in forward and reverse-acting varieties by using either the "zero" or the "one" output of the preceding stage to drive the next stage. Other counting sequences can be obtained by having some stages counting in the forward and others in the reverse direction. It is shown that if one of the outputs is used to reset the counter to zero any scaling rate up to 2^n for an n-stage counter can be realized. Using relays or electronic gates for the output selection, the scaling rate can be controlled automatically. Some examples are given of a possible application of this type of counter to automatic division of two numbers using the divisor to control the scaling rate and feeding the dividend into the counter itself. The problem of rounding-off in this case is also discussed. The numbers handled by this type of counter being essentially represented in the scale of one, its use for this purpose in automatic digital computers will be limited by speed considerations. Decimal counting is another possible application, though the fact that the intermediate states of the counter are not easily identified may be an objection in some cases.

B. J. Loopstra

55-146

A Decade Frequency Divider—R. B. Mebsby. (*Elect. Engrg.*, vol. 27, pp. 295–298; July, 1955.) A frequency divider developed for use with quartz crystal clocks is described. The Eccles-Jordan is the basic circuit. The first divider is designed to operate over the range of 20 cycles to 100 kc.

R. G. Canning

55-147

Cold-Cathode Counting Circuits—H. L. Foote. (*Comm. and Elect.*, No. 18, pp. 161–164; May, 1955.) Three-electrode cold-cathode gas tubes have been employed to form counting circuits. Both binary and decimal counters have been developed, and six different circuits are shown and described. The counting speeds which have been achieved are from 100 to 700 pulses per second for the different configurations.

R. K. Richards

55-148

An Inexpensive Dekatron Scaler—G. A. Kerkut. (*Electronic Engrg.*, vol. 27, pp. 378–379; September, 1955.) The circuit is given of an inexpensive (about $75.00) gas-tube scaler for use in nerve physiology. A total count of up to seven figures is possible, using gas tubes and a electro-mechanical counter.

R. G. Canning

621.318.57:621.38 55-149

Multi-Electrode Counting Tubes—K. Kandiah and D. W. Chambers. (*Jour. Brit. IRE*, vol. 15, pp. 221–232; April, 1955. Discussion, p. 232.) Applications other than straightforward counting operations are discussed for decimal counting tubes of various types. The design of a pulse amplitude analyzer using trochotrons and dekatrons in a matrix system is outlined. Life of tubes is comparable to that of ordinary tubes.

Courtesy of PROC. IRE and *Wireless Engineer*

55-150

The Design of Hard-Valve Binary Counters—D. M. Taub. (*Electronic Engrg.*, vol. 27, pp. 386–392; September, 1955.) A simple binary counter circuit (Eccles-Jordan) is considered, and typical calculations are shown for designing the circuit to operate satisfactorily under the conditions of component and supply voltage variations encountered in practice. The method is valid at counting speeds up to several kilocycles per second.

R. G. Canning

55-151

A High Speed Decade Counter Using Germanium Diodes in the Feedback Loops—H. R. Joiner and D. R. Woodward. (*Electronic Engrg.*, vol. 27, pp. 404–405; September, 1955.) A description is given of a simple decade counter which will operate at frequencies of up to 500 kc. The circuit uses four 12AU7 tubes and two crystal diodes.

R. G. Canning

55-152

Quarterly Report No. 7, Second Series—J. R. Bowman, A. Milch, *et al.* (*Quart. Rept. Computer Components Fellowship Mellon Inst.*, 70 pp.+x; April 1, 1955 to June 30, 1955.) Part I of this report, "Printed Circuits," contains, in two of its three sections, some detailed descriptions of methods of forming two dimensional circuit elements (resistors, capacitors, and busses) that will operate satisfactorily at temperatures over 200°C. Thus far vacuum evaporated capacitors using a silicon monoxide dielectric, and resistors formed by spraying antimony-doped tin chloride solution in acetone onto a pyrex plate held at elevated temperatures, have been most satisfactory. Due to the need for accurate measurements on these films, a third section is devoted solely to a review of the instrumentation available in the field of film thickness measurements and profilometry. Part II, "Electroluminescence," carries forward the work on dielectric embedded and chemically deposited electroluminescent films. Also included is a section on thermoluminescence measurements on chemically deposited films of manganese-activated zinc sulfide in which three distinct glow peaks are noted.

A. Milch

DIGITAL SYSTEMS RESEARCH

681.142 55-153

System Design of the SEAC and DYSEAC—A. L. Leiner, W. A. Notz, J. L. Smith, and A. Weinberger. (TRANS. IRE, vol. EC-3, pp. 8–23; June, 1954.) This article discusses some of the factors which governed the choice of system features in the SEAC and DYSEAC and describes some of the standard procedures which were developed for working out their system designs. These included the development of system specifications, functional plans, and finally the development of wiring plans. The choice of system specifications is described where the effort was to achieve a balance among the principal memory, switching, and external communications units whose characteristics were widely varied. The wiring for the DYSEAC, carried out by relatively inexperienced technicians, led to the preparation of three distinct types of working plans of which an example of each is given. The production of wiring plans for new computer systems by existing digital machines is suggested and treated briefly. (See **55-62** of June, 1955; and **55-106** of September, 1955.)

A. S. Hoagland

55-154

Automatic Square Rooting—E. H. Lenaerts. (*Electr. Engrg.*, vol. 27, pp. 287–289; July, 1955.) A method is described by which automatic square rooting can be incorporated in a computer of the LEO type. By this method, the time required to find the square root of a 40-bit number is reduced to 6.4 mc as compared with 80 mc using programming. The bits are marked off in groups of two, and the method is similar to the traditional decimal square root process taught in high schools.

R. G. Canning

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DIGITAL EQUIPMENT

681.142 55-155

Computer for Universal Application—(*Elec. Times*, vol. 127, pp. 319–320; February 24, 1955.) Brief description of DEUCE, a commercially available computer developed from the ACE; it has punched-card input and output systems, mercury delay lines for short-term storage and a magnetic recording drum for long-term storage. The total floor space occupied by the equipment is 14 feet by 4 feet 6 inches.

Courtesy of PROC. IRE and *Wireless Engineer*

55-156

Engineering Description of the Electro-Data Digital Computer—J. C. Alrich (TRANS. IRE, vol. EC-4, pp. 1–10; March, 1955.) The data-processing system described in this article is composed of six units: an electronic digital computer, a control console, a typewriter control unit, a punched card converter unit, a magnetic tape auxiliary storage unit, and a power control unit. The computer is a binary coded-decimal 1-2-4-8 single address, fixed decimal point, magnetic-drum, stored-program machine. Decimal digits are transferred serially, bits of a digit are transferred in parallel. The word length is ten digits and sign. The drum stores 4,000 words in the main memory and 80 words in four 20-word quick-access loops. The maximum access time in these loops is 1.69 milliseconds, 1/10 of the access time in the main memory. These loops are designed to block transfer 20 words to or from any section of the main memory. The accumulator register may transfer a single word to or from a quick-access loop. The computer has a repertoire of 55 commands. Program modification can be carried out automatically by means of a special four-digit B-register. This feature reduces the number of commands necessary to accomplish a given result. In floating point operations, the number in the A-register can be normalized and the number of left shifts tallied in a special counter. The machine timing cycle and adder section operations are clearly described. Marginal checking facilities have been designed into the equipment; however, self-checking features have not been included in the design. A description of the auxiliary tape unit is not included in the article. Its capacity is stated as 160,000 words. The system contains 1,525 vacuum tubes and 3,809 germanium diodes.

Raymond Davis

55-157

A Commercial Electronic Calculator—W. Woods-Hill. (*Elect. Engrg.*, vol. 27, pp. 332–337; August, 1955.) A brief description is given of the British Tabulating Company types 542, 550, and 555 calculators. The 555 employs some 1,300 tubes, magnetic drum storage (100 words), Hellerith card input-output, and provides 120 program steps. The drum uses a helix of 0.004 in stainless steel wire instead of oxide coating.

R. G. Canning

55-158

Characteristics of a Logistics Computer—Eugene Leonard. (*Proc. WESCON Computer Sessions*, August 25–27, 1954, Los Angeles, Calf., pp. 77–85; 1955.) This paper presents the basic characteristics of the ORDFIAC, a computer built for the Ordnance Department of the Army by the Electronic Computer Division of the Underwood Corporation. The ORDFIAC is a completely serial, decimal, magnetic drum calculator of conventional design and moderate speed. It features an extremely large magnetic drum memory of 10,000 words contained in 100 relay selected memory channels. It uses a three-address command structure and possesses a conventional instruction list plus a square root command and a special repeat multiply and sum command developed for matrix operations. The machine is designed around an IBM punched card as input-output media. Checking circuitry is provided to catch certain types of machine failures. In particular, emphasis is placed on insuring correct channel selection in memory system.

Myron J. Mendelson

55-159

An Input-Output System for a Digital Control Computer—L. P. Retzinger, Jr. (*Proc. WESCON Computer Sessions*, August 25–27, 1954, Los Angeles, Calif., pp. 67–76; 1955.) The computer under discussion requires inputs in serial binary form, least significant digit first, representing several different shaft positions. Binary-coded commutator discs, having double sets of pick-off brushes to avoid ambiguity, are used for the purpose. The logical details of the anti-ambiguity circuitry are described, and a scheme is presented which allows much of this circuitry to be time-shared among all digitizers. Similar digitizers are used to monitor the output shafts of the system. The computer itself, a serial binary digital differential analyzer, generates in binary form the difference between the desired position and the actual position as indicated by the digitizer. This difference is read into a group of flip-flops once per drum revolution of the computer. The flip-flops hold the number long enough to charge a capacitor to a voltage which is proportional about the origin over the range of $+7$ to -8 units and levels off on either side. The capacitor voltage then serves as a servo error signal, driving a motor to bring digitizer to desired position. Flip-flops and associated decoding network are time-shared among several similar output servos.

E. C. Johnson

55-160

Numerical Control of Machine Tools—Leroy U. C. Kelling. (TRANS. IRE, vol. IE-2, pp. 3–8; March, 1955.) After a discussion of several aspects of numerical controls as applied to machine tools, this paper describes the specific application to a large turret punch press. In response to control information supplied by punched cards, the work table of the press is positioned in two directions, the turret rotated to the correct tool, and the punch mechanism actuated. The cards, one for each punching operation, are read automatically to guide the machine through a sequence of any desired length. "The operating times of the complete positioning and punching cycles vary from 2 to 8 seconds, depending upon the distances moved."

E. C. Johnson

55-161

A Digital Computer for Use in an Operational Flight Trainer—W. H. Dunn, C. Eldert, and P. V. Levonian. (TRANS. IRE, vol. EC-4, pp. 55–63; June, 1955.) The requirements on a digital computer for use in an operational flight trainer are presented. Programming of the flight equations for available general purpose digital computers showed that none of them could perform the required calculation fast enough. A digital computer that has an instruction code designed to meet the special requirements of real time flight simulation is described. It makes use of conventional memory devices and switching techniques. Speed is achieved by means of appropriate logical organization.

E. C. Nelson

55-162

Magnetic Memory Device for Business Machines—S. J. Begun. (*Elect. Engrg.*, vol. 74, pp. 466–468; June, 1955.) This is a general description of the Tape DRUM magnetic storage device. Information is recorded on an endless magnetic tape from 10 to 12 inches wide and from 8 to 450 feet long. The length of the tape is divided into a series 18 inch "pages" of recorded information, the pages being separated by an unrecorded section of one inch. A desired page is positioned wrapped around half of a 1200 rpm rotating drum of 12-inch diameter. The portion of tape in contact with the drum is scanned by a line of magnetic heads inside of the drum with their gaps aligned and pole pieces extending slightly above the drum surface. Signals from the heads are brought out via slip rings. Ten channels per inch are provided, and the cell density in one channel is 100 bits per inch. The system has a storage capacity of 60×10^6 bits on a 450-foot tape, with a maximum access time of 30 seconds. The page index system is described, and a random-access version of the system is described. The article does not describe the electronic circuitry for reading, writing, and switching.

Harry T. Larson

55-163

Control Features of a Magnetic-Drum Telephone Office—W. A. Malthaner and H. E. Vaughan. (TRANS. IRE, vol. EC-4, pp. 21–26; March, 1955.) The DIAD telephone system to which this article refers uses information storage and processing techniques similar to those used in computers. Knowledge of the condition of the external lines and of the occupancy of the connecting switches is continuously available on magnetic drum records. The system demands the storage and transfer of this information during the process of setting up a call by the exchange control circuits. In the article, selected control features are illustrated by block schematic diagrams, and although the interconnection of the controls and the conversation path switches is not specifically described, the features selected for description are sufficient to indicate the possibilities of the use of common control techniques with magnetic drum storage for the control of telephone and other switching systems requiring the assembling and processing of data. (See **54-87** of June, 1954.)

S. W. Broadhurst

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—*The Editor*

55-164
Photoelectric Reader Feeds Business Machines—D. H. Shepard and C. C. Heasley, Jr. (*Electronics*, vol. 28, pp. 134–138; May, 1955.) A machine built by the Intelligent Machines Research Corporation photoelectrically reads printed characters and generates pulse codes representing these characters. These coded characters may then be handled by conventional electronic business machines. The machine called the analyzing reader inspects the characters at a rate of 1,600 words per minute and recognizes the unique combination of strokes which make up a character. A small special computer which forms a part of the analyzing reader converts these unique stroke combinations into pulse codes representing the characters. This article describes the process of reading characters from a printed page and determining the stroke combinations. Both block and schematic diagrams are shown of the equipment necessary for reading characters, eliminating background noise and generating stroke combinations. A simplified block diagram of the computer or interpreter is shown.

Norman F. Loretz

55-165
The Automation of Bank Check Processing—R. Hunt Brown. (*Computers and Automation*, vol. 4, pp. 6–9, 16; August, 1955.) The problems of standardization and preprinting or prepunching of checks are two of the most difficult problems in establishing an automation procedure for a bank. The author describes three machines which are able to read preprinted information for processing standardized checks. It is suggested that these readers could be used with a system similar to the one outlined for savings banks in the July issue. (See **55-168**, this issue.)

Gordon Morrison

UTILIZATION OF DIGITAL EQUIPMENT

55-166
Numerical Representation in Fixed-Point Computers—Beatrice H. Worsley. (*Computers and Automation*, vol. 4, pp. 10–13; May, 1955.) The restrictions of a fixed-point machine and the methods of surmounting the resulting difficulties are presented at an elementary level for the person unfamiliar with scaling and floating point operation. Some brief attention is also given to the topic of compiling routines.

Gordon Morrison

81.142 55-167
Effectiveness of Two-Step Smoothing in Digital Control Computers—Robert E. Spero. (PROC. IRE, vol. 41, pp. 1465–1469; October, 1953.) The basic problem is that of noise elimination from a signal. Given a known input signal containing noise, eliminate the noise from the output by smoothing. Smoothing is a function of N, the number of observations per second and T, the smoothing time. The larger N and T are, the better the smoothing. However, if both N and T are large (say $N=400$ obs/sec and $T=20$ sec.) the data handling problem is difficult, if not impossible. Spero shows that a two-step procedure used in series can overcome the above trouble. The two steps involve first sampling at a high rate for a short time and second, sampling the adjusted data at a slower rate over a longer time. Examples are given for smoothing under three different conditions (weight factors). 1) the weight factors are weighted averages; 2) the weight factors are a geometric series; and 3) the weight factors give a special form of second-order smoothing. A basic assumption in the development of the smoothing techniques described in this article is that the form of the basic input signal is known. The author assumes that the data to be smoothed consist only of random noise. If this is not the case, the assumption of zero autocorrelation breaks down and hence the smoothing technique.

G. Mayle

55-168
The Application of Automatic Computing Equipment to Savings Bank Operations—R. Hunt Brown. (*Computers and Automation*, vol. 4, pp. 18–21; July, 1955.) The author feels that the banking profession has issued a call for assistance from the automation field. This article presents his suggestion in general terms for a system which would be suitable for application to savings bank operations. The significant aspect of this system is that it provides all the paper records provided by current hand systems. (See **55-165**, this issue.)

Gordon Morrison

55-169
Reliability in Electronic Data Processors—William B. Elmore. (*Computers and Automation*, vol. 4, pp. 6–9, 38; May, 1955.) A few experiences with current commercial electronic data processors have been brought together to give sketchy indication of the dependability of such equipment and of the reliability of the results obtained by its use. Unfortunately, the examples chosen have been selected to indicate the ultimate reliability to be expected rather than the typical reliability.

Gordon Morrison

55-170
Computer-Programmed Preventive Maintenance for Internal Memory Sections of the ERA 1103 Computer System—Seymour R. Cray. (*Proc. WESCON Computer Sessions*, August 25–27, 1954, Los Angeles, Calif., pp. 62–66; 1955.) The ERA 1103 is a general purpose digital computer employing a two-address type of instruction. The storage systems consist of a 1024 word electrostatic storage (CRT), a 16,384 word drum, and 200,000 words of magnetic tape storage on four tape units. External magnetic tape and punch card mechanism provide additional storage. Individual addressing of the electrostatic and drum storage provides a total of 17,408 registers directly addressed. Since the CRT storage does not act as a buffer for the magnetic drum storage, it is possible to test each system as an isolated unit. Preventive maintenance is scheduled at the beginning of every eight-hour period of operation. The prepared programs examine the performance of each portion of the system while abnormal operating conditions are imposed on the portion under test. The programs are designed to indicate, by means of the monitoring typewriter, the location of any faults. Failures in the arithmetic part of the system are indicated on a neon-light panel. Marginal checks used are: 1) Reduced filament voltage, from 6.3 to 5.5 volts; 2) power supply variations, in which the eight power supplies are varied sequentially over a 20 per cent range about the normal; and 3) threshold clipping levels, which may be raised or lowered by special equipment provided for the purpose. The electrostatic storage is tested by a cycle test, checking access control circuitry, deflection circuits, and normal storage properties, and a reference test, which checks read-around ratio. The author describes the patterns used in some detail, as well as the manner in which the patterns are processed through the memory. The drum storage test includes 16 reading and 16 writing references to each of the 16,384 addresses on the magnetic drum. Various combinations of digits are used to simulate operating conditions. A summary of operational results for six months experience on an 1103 computer concludes the paper. It is interesting to note that in this period the production time increased steadily from 61 per cent to 82 per cent, and the preventive maintenance dropped from 30 per cent to 14 per cent, an indication of the excellence of the program.

F. H. Hollander

55-171
The Digital Computer as a Laboratory Tool—Arthur L. Leob and Harry H. Denman. (*Jour. Soc. Ind. and Appl. Math.*, vol. 3, pp. 1–16; March, 1955.) This paper deals with the use of Whirlwind I, an electronic digital computer at M.I.T., for the computation of optical constants of thin metal films. The mathematical problem involved is that of solving a system of two transcendental equations. An iterative method is used. Some description of the Whirlwind Computer and its programming is included.

T. H. Southard

55-172
Computers and Weather Prediction—Bruce Gilchrist. (*Computers and Automation*, vol. 4, pp. 8–9; March, 1955.) A brief history of the use of numeric methods for weather prediction is presented together with an estimation of the requirements to be satisfied by a digital computer which could be used in the preparation of weather forecasts.

Gordon Morrison

BOOK REVIEWS

55-173
Minds and Machines—W. Sluckin. (Penguin Books, Ltd., London, 223 pp.; 1954.) The various subjects that fall under the head "communication and control" have advanced so rapidly during the past decade that it is hard to keep even moderately well informed as to what is happening in this sphere of knowledge. This book performs a useful task in unifying and explaining in more or less everyday language the results of several different branches of research; automatic computers, brain physiology, thought processes, homeostasis, self-adapting mechanisms and the like. The author, trained both as an electrical engineer and as a psy-

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—*The Editor*

chologist, is well qualified to survey the ield. Some of the topics are dealt with less fully than one might have expected or hoped; for example, the intricate ideas of informa- tion theory are treated perfunctorily. But on the whole the discussion is sound and clear and the book is unusually successful in explaining how the study of certain complex machines has enlarged understanding of the behavior of the brain and influenced the science of psychology.

Courtesy of *Scientific American*

55-174

Les machines à penser—Louis Couffignal. (Le Editions de Minuit, Paris, 158 pp. +4 plates; 1952.) The development of large and complex electronic computing machines naturally excites a great deal of popular interest. Words such as memory, decision, instruction, information and language are often used in descriptions of these machines. There are strong objections to the use of such anthropomorphic notions as that electronic digital computors possess rudimentary powers of scholarship, volition or reasoning. But it really all reduces to the definitions used. The meaning of such definitions would be unnecessarily narrowed down and their pictorial power lost if processes like memory or reasoning were attributed solely to human beings. Louis Couffignal is not afraid of using anthropomorphic terms, provided it is understood that the machines achieve the same ends by quite different means. The book opens with definitions of a machine and of thought. If one defines a machine as an assembly of objects which are put together in such a way that they replace man in the execution of a set of operations proposed by man, then, naturally, even the simple adding machine possesses a rudimentary memory and its mechanism of "carry-over" replaces quite a complex set of mental operations of a human brain. A description of adding machines and punched-card machines follows. It does not go into great technical detail of the machines themselves, but is sufficient to convey a general idea of their capabilities. The description of the universal machines deals with Babbage's ideas, with Mark I of Professor Aitken, ENIAC, and a machine built at the Institut Blaise Pascal. The advantages of the binary system are clearly shown; its adoption leads to the reduction of the size of a large machine of a given capacity to about a third—a very considerable saving. The operations of multiplication, division, and square-root extraction, using the binary system, are well explained. The next chapter is concerned with analog machines, such as the differential analyzer of Vanevar Bush; it is a pity that the electronic analogue machines, such as Pepinsky's X-RAC, are not mentioned. The chapter dealing with the nervous system is rather superficial; one has the feeling that the writer is not in his own field here. Surely modern work on giant nerve fibers of squids and the permeability changes of the nerve membranes to potassium and sodium ions could have been included. The analogy between the transistor and a synapsis may not be as close as the author seems to believe. In the chapter on the mechanization of logic the author, who is the director of the computing laboratory of the Institut Blaise Pascal, is much more in his element. The expression of logic in a binary system is of great interest, although rather heavy going for a lay reader. It took me some time to discover what the symbol 0010.0100 for a logic function (p. 105) really means and what is the significance of the dot in the symbol. Further confusion results from designations of "prédicats" P_n by a capital letter on p. 104, by a lower-case p_n on p. 112 and a capital in Fig. 25. Further, a function $p_n=0000.1111$ on p. 109 has n as a subscript, and p^{n+1} on p. 114 has it as a superscript, without adequate explanation. However, these are only minor defects which do not detract from the value of the book as a suitable introduction to the subject. The book finishes with, not conclusions, but a programme of research, stimulated by the close analogies between processes of human thought and modes of action of modern computing machines. There are no references and no subject index.

V. Vand

Courtesy of *Nature*

55-175

Analog Methods in Computation and Simulation—Walter W. Soroka. (McGraw-Hill Book Co., New York, 380 pp., 9 p. index+xii, Illus.; 1954.) This book describes various electrical and mechanical components which (ideally) obey fundamental mathematical laws, and proceeds to demonstrate how computers and simulators may be constructed from these basic building blocks. The chapters are: "Mechanical Computing Elements"; "Electromechanical, Electrical, and Electronic Computing Elements"; "Machines for Simultaneous Linear Algebraic Equations"; "Analog Solution of Nonlinear Algebraic Equations"; "The Mechanical Differential Analyzer"; "Electronic Analog Computers (Electronic Differential Analyzers)"; "Dynamical Analogies"; "Equivalent Circuits for Ordinary and Partial Differential Equations in Finite Differences"; and "Membrane and Conducting-sheet Analogies." The analog computer has both a long history and a current vitality. The basic precepts may be quickly enumerated, but a feeling for the subject is developed only through acquaintance with a wide spectrum of examples, many in the "ingenious device" category. Professor Soroka has provided these examples in profusion, yet without making the book a mere catalog of miscellany. He has done a good job of collecting and organizing material largely available heretofore only in isolated spots. The book is descriptive, but the author does not hesitate to "put the numbers in." The problem of scaling receives adequate attention throughout the book, and the technical limitations of many of the computers described are indicated. A particularly valuable addition would have been the expansion of the brief chapter on electronic analog computers to include checking procedures and error analysis techniques. The author's preface indicates that the book is considered a textbook; however, no exercises for the student are included. Properly employed, it could form the basis for a course at perhaps a high undergraduate level, although appreciation of the fine points in certain chapters requires somewhat more advanced training. Laboratory work would be essential, and might well be modeled upon examples in the book. The practicing engineer will find this a useful basic reference, but one which does not attempt to solve his practical problems of detail design to meet space and weight limitations or to ensure reliable operation under adverse environmental conditions. In this connection, the reader will be grateful that the book contains a wealth of basic references to the literature.

Louis B. Wadel

Courtesy of PROC. IRE